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Effect of Passivation Film Stress on Shift in Threshold Voltage of GaAs FETs

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Abstract

GaAs FETs are widely used for high-speed and low-power devices, especially in optical communication systems. To improve product reliability, it is very important to control mechanical stress in device structures. This is because that the stress field changes the dopant distribution[1] and shifts electronic characteristic of devices[2]-[5] due to piezoelectric effect. There are several stress development processes in the device manufacturing, such as thermal stress due to mismatch in thermal expansion coefficients among thin film materials used in the device structure and intrinsic stress which occurs during film deposition. To evaluate precise stress fields in actual device structures, the authors have developed stress simulation methods based on finite element analysis, a measurement method for mechanical properties of thin films, and a microscopic stress measurement method[6]. To improve product reliability of silicon devices, it is confirmed that these methods are effective for control or optimization of mechanical stress fields in the device structure[7][8]. In this paper, the stress evaluation methods are applied to discuss the effect of passivation film stress on the shift in threshold voltage of GaAs FETs.

Fig. 1 shows basic structure of the stress evaluated model. Tungsten and Tungsten-silicide were used for gate electrode material. Silicon-dioxide film was deposited for passivation on the GaAs substrate and the epitaxial layer by chemical vapor deposition. The internal stress of the oxide film was varied from -200 MPa to 800 MPa by changing gas pressure during the film deposition. The internal stresses of the tungsten and tungsten-silicide films were almost constant at about 1000 MPa. The process-induced stress in the GaAs substrate was analyzed by a two-dimensional finite element method[7]. The predicted shear stress distribution in GaAs substrate after the deposition of the passivation film of which the stress was about 800 MPa is shown in Fig. 2. It is clear that stress concentrates near the gate edge. In this case the maximum stress at the substrate surface reaches about 240 MPa.

The shift in threshold voltage of the FET was analyzed by considering stress-induced piezoelectric charge. The basic idea was modeled by Asbeck et al.[2]. The piezoelectric charge distribution can be calculated by the following equation.

$$\rho = \nabla \cdot \mathbf{P} = d\left\{\frac{d\tau_{zx}}{dx} - \frac{1}{2}\frac{d\sigma_x}{dz} + \frac{1}{2}\frac{d\sigma_z}{dz}\right\} \qquad (1)$$

Here, d is piezoelectric constant of 2.6×10^{-12} Coulomb/N, σ_x, σ_z are normal stress components along x-axis and z-axis shown in Fig. 1, respectively, and τ_{xy} is shear stress component. The charge induced by mechanical stress is determined by not the absolute value but the stress gradient. Fig. 3 shows a example of the predicted charge distribution ρ_x ($=dP_x/dx$) at the gate edge along the depth direction. The piezoelectric charge mainly develops near the substrate surface within 100 nm. The

maximum value at the surface is about $1x10^{17}/cm^3$. The threshold voltage shift is calculated by integrating the charge in the substrate under the gate electrode.

$$\delta V_{th}=\frac{d}{\varepsilon}\int\int z\{\frac{d\tau_{zx}}{dx}-\frac{1}{2}\frac{d\sigma_x}{dz}+\frac{1}{2}\frac{d\sigma_z}{dz}\}\,dzdx \qquad (2)$$

The predicted shift in the threshold voltage of the FET is compared with the measured data in Fig. 4. The abscissa is the stress in the passivation films and the ordinate is the threshold voltage shift. The predicted value is about 0.1 volts and it agrees well with the measured data. In this case, the magnitude of the shift can be minimized by using the passivation film with a compressive stress of about 50 MPa. Thus, it is concluded that the shift in the threshold voltage of GaAs FETs due to process-induced stress can be analyzed quantitatively by stress simulation with a consideration of the internal stress of thin films used in the FET structure.

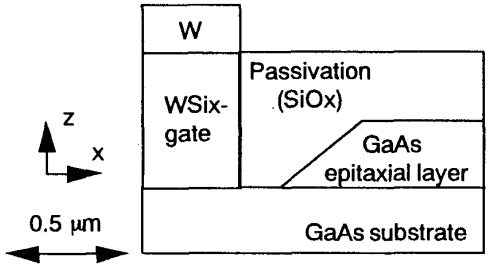

Fig. 1 Model structure of GaAs FET

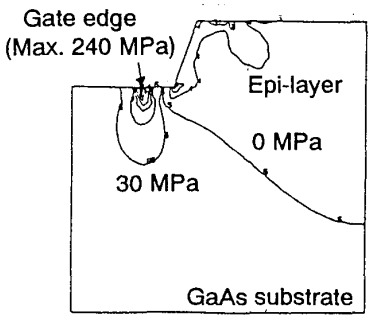

Fig. 2 Predicted stress distribution in GaAs substrate

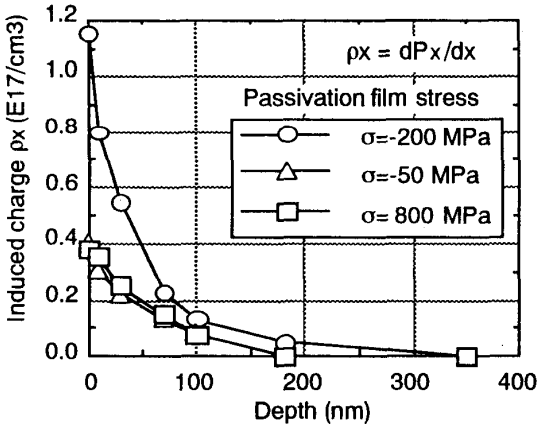

Fig. 3 Piezoelectric charge distribution at gate edge

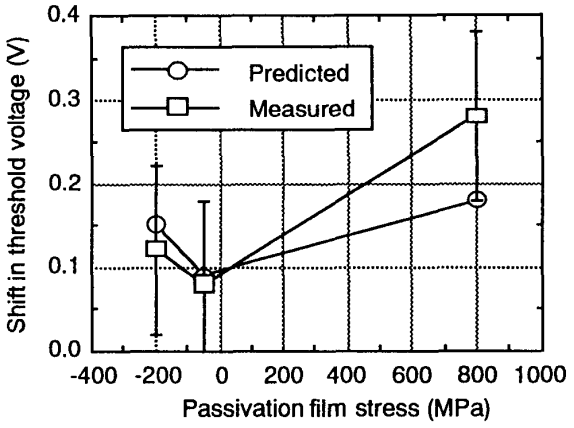

Fig. 4 Threshold voltage shift due to passivation

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