2-1 (Invited)

Inverse Modeling Profile Determination: Implementation Issues and Recent Results

N. Khalil and J. Faricelli

Digital Semiconductor
77 Reed Road, HLO2-3/J09
Hudson, MA. 01749, USA
Tel: (508)568-7218
Fax: (508)568-4681

1. Introduction

Since we first reported on the inverse modeling technique to determine one- and two-dimensional doping profiles of a MOSFET [1,2], we have had considerable success in using the method. The procedure has become an essential component in our TCAD characterization efforts. In this paper, we first present a recent object-oriented implementation based on the Tcl/Tk toolkit [3]. We then discuss enhancements and adaptations to MINIMOS [4] to make it more suitable as a Poisson solver for capacitance calculation. We also investigate the use of V_{th} data instead of inner sidewall capacitance data to determine the 2D channel doping and elaborate on the merits and limitations of this approach. Finally, we show recent results that illustrate the applicability of the method for the characterization of deep submicron technology, and the importance of accurate 2D doping profiles for device simulation.

2. Implementation Issues

To allow for the general use and automation of the extraction code, we implemented an object-oriented command language interface based on the Tcl/Tk toolkit [3]. A set of TCAD objects forms the foundation of the interface. For example, a *Model Object* (MO) is an encapsulation of model data such as name, variable information, and the computational body that implements its input-output relationship. Analysis task programs are integrated as MO methods: A `FIT` method invokes the nonlinear least-squares optimizer to minimize the sum of squares fit criterion between calculated outputs and experimental values [5]. Two types of objects exist: mathematical (e.g. Spline functions with interpolating and least-squares approximation methods) or physical (e.g. MOS capacitor with various capacitance measurement methods).

We also modified MINIMOS [4] to adapt it to the requirements of the inverse modeling technique. Several improvements were made to the base MINIMOS5 code to improve the accuracy of capacitance simulations, including a correction to the shape of the inversion/accumulation layer carrier distribution due to quantum mechanics [9] and extensions to handle more elaborate gate geometries [12]. For computational efficiency, we

implemented a Poisson-only solution mode, a VARY statement to compute capacitances from derivatives of the space charge, and coded a callable interface to reduce the overhead involved with invoking an external simulator. Implementation of these changes reduced the computation time roughly in half. In addition to performance improvement, the use of the VARY statement, which freezes the solution grid, eliminates some of the numerical errors associated with capacitance calculation by differentiation. We also added an additional adaptive gridding strategy specific to simulations of the MOS device capacitances. MINIMOS's adaptive gridding strategies are targeted at gridding issues related to carrier transport. We found that, to obtain accurate and smooth simulated area and periphery source/drain diode capacitances, it was necessary to add grid lines far from the flow of carriers. Numerical experiments showed that it is most effective to add a few grid lines along the edges of the depletion region on the bulk side of the source/drain junctions. Accordingly, we implemented a regrid on the gradient of the space charge, normalized by the doping. Control points (e.g. 0.1 and 0.9) were used to define the "edge" of the depletion region. By using this definition, rather than a simple regrid on the gradient of the space charge, we avoid adding excessive grid in the inversion or accumulation regions, where the gradient of the space charge is much higher than along the depletion region edge.

3. Extraction from V_{th} vs V_{bs} data

Analytical expressions for extracting the doping profile of a MOSFET from V_{th} vs V_{bs} data has been proposed independently by Shanon [6] and Buehler [7]. Recently, Hayashi et al. [8] used inverse modeling and B-splines representation to extract the channel profile from V_{th} and its body effect. We have started investigating the extraction of 1D and 2D MOSFET profiles from constant current threshold data at varying bulk and drain bias.

To assess the accuracy of this approach, we extracted the 1D doping profile of a long channel MOSFET from V_{th} vs V_{bs} data and compared it to the profile extracted from deep depletion capacitance data. The same knot sequence determined as in [10] was used in both cases. As seen in Fig. 1, the two profiles agree reasonably well. The maximum difference between the two profiles occur near the interface. This can be attributed to the following two reasons: First, the inability of the V_{th} data to resolve the profile within the initial depletion region, even when using small forward bias points; Second, the inability of the high frequency deep depletion measurement to detect interface trap charges which have a slower response time. Indeed, one can take advantage of this fact to determine a uniform interface charge density value (d_{it}) by matching quasi-static capacitance measurement with simulation using a profile extracted from deep depletion data. The d_{it} value determined by this procedure is in good agreement with the value determined by charge pumping measurement.

For the 2D case, we investigated the use of threshold voltage data as a substitute for the inner sidewall capacitance in determining the profile. The use of the threshold data alleviates some of the measurement difficulties associated with capacitance measurement. Furthermore, since V_{th} measurements can be collected on a regular device, special test structures, that eliminate capacitive coupling effects, are not necessary. We note that gate capacitance measurement are still required to determine the profile variation in the extended source/drain region. Although some profile information can be extracted from the threshold data, an exact profile reconstruction is not possible in all cases. This is illustrated in Figure 2 which shows the result of a numerical experiment where the

channel 2D profile was extracted using V_{th} data in one case, and inner sidewall capacitance in the other. In both cases, the same known doping profile was used to generate simulation data for the extraction. We note that the initial profile has a non-uniform lateral doping variation near the Si/SiO_2 interface similar to that extracted from devices with reverse short channel effects. As illustrated, the profile extracted from the capacitance data is in good agreement with the initial profile, whereas the one extracted from the V_{th} data cannot detect the dopant pile-up near the source/drain junction.

4. Recent Results

In Figure 3, we show simulated and experimental quasi-static C–V data for our next generation technology. The oxide thickness is 45 $\AA$ as determined from accumulation capacitance measurement [11]. The agreement between experimental and simulated values is good. This clearly indicates that the physical models used in the simulation are valid for thin oxide devices including the first order quantum mechanical correction.

Finally, in order to illustrate the importance of 2D profiles for accurate device simulation we compare I–V simulation using an extracted profile with experimental data. Besides minor adjustments to allow for the effect of series resistance (R_T), and the interface charge (N_{SS}), we use default parameters including mobility parameters identical to those calibrated for long channel devices on older technologies. We note that we determined L_{poly} and the doping concentration in the polysilicon gate from capacitance measurements as in [12]. Figure 4 illustrates the excellent fit achieved for the I–V characteristics.

5. Conclusion

In this paper, we presented a new implementation of the inverse modeling profiling technique. We also described preliminary investigations into the extension of the method to use V_{th} data in the extraction procedure. Finally, we showed recent results that demonstrate that the method is suitable for characterizing state-of-the-art modern technology.

References

[1] N. Khalil, et. al., *Digest Symposium VLSI Technology*, pp. 131-132, 1994.

[2] N. Khalil, et. al., *IEEE Electron Device Letters*, 16(1), pp. 17-19, 1995.

[3] J. K. Ousterhout. *Tcl and the Tk Toolkit* Addison-Wesley, Reading, Massachussets, 1994.

[4] *MINIMOS 5 - User's Guide*, Institute of Microelectronics, Technical University of Vienna, Austria, 1991.

[5] N. Khalil. *ULSI Characterization with Technology Computer-Aided Design.* PhD thesis, Technical University of Vienna, 1995.

[6] J. M. Shannon. *Solid-State Electronics*, 14, pp. 1099-1106, 1971.

[7] M. G. Buehler. *Applied Physics Letters*, 31(12), pp. 848-850, 1977.

[8] H. Hayashi, et. al., *42nd Japanese Applied Physics Annual Meeting*, 28a-TF-4, p. 1347, 1995.

[9] W. Hänsch, et. al., *Solid State Electronics*, 32, pp. 839-849, October, 1989.

[10] N. Khalil, et. al., *proceedings ESSDERC*, pp.191-194, 1995.

[11] R. Rios and N. D. Arora, *IEDM Tech. Digest*, pp. 613-616, 1994.

[12] C.L. Huang, et. al., *IEEE Trans. Electron Devices*, June 1996.

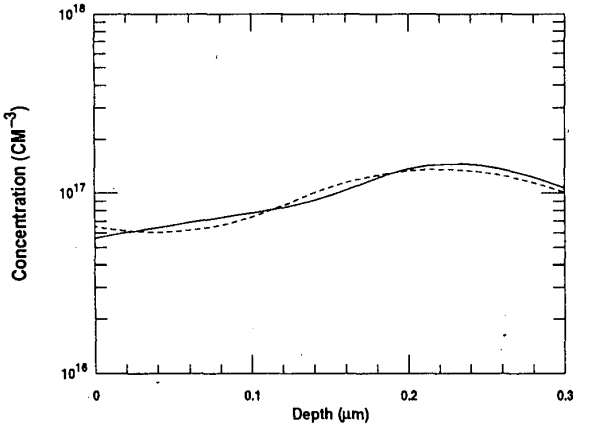

Figure 1: Comparison of proflies extracted from V_{th} vs V_{bs} data (solid) and from deep depletion capacitance (dashed). (T_{ox} = 65Å, W = 40 μm, L = 40 μm).

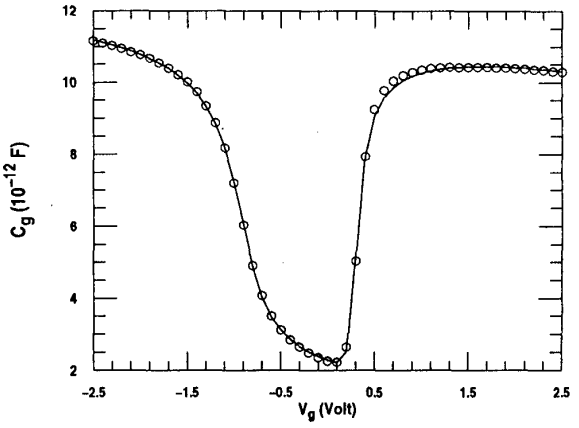

Figure 3: Experimental (symbols) and simulated (solid line) quasi-static capacitance data, (T_{ox} = 45Å, W = 40 μm, L = 40 μm).

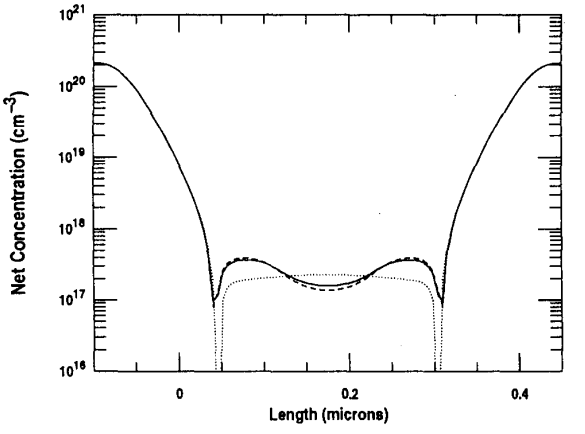

Figure 2: Original (solid), extracted from V_{th} (dotted) and from capacitance data (dashed) net doping profiles at the Si/SiO_2 interface for the simulation experiment (L_{poly} = 0.35 μm).

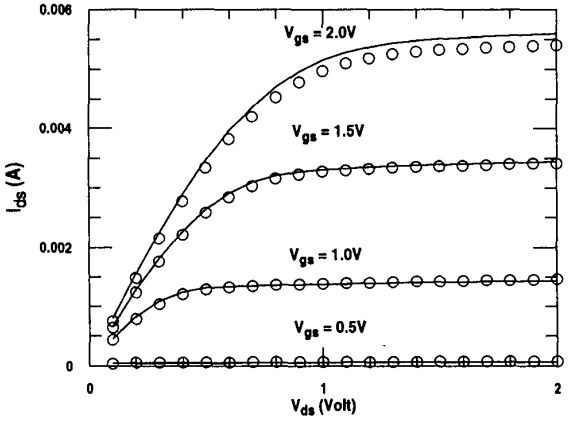

Figure 4: Comparison of experimental (symbols) and simulated (solid lines) I_{ds}–V_{ds} at different V_{gs}. (T_{ox} = 45Å, W = 14 μm, L_{poly} = 0.31 μm).