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Simulations of the forward behaviour of hybrid Schottky-/pn-diodes

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Abstract

Device simulations of a hybrid diode – an integrated combination of a Schottky diode and a pn-diode – are presented. It is shown that under low forward bias the device acts like a Schottky diode, while under strong forward bias the behaviour turns into that of a pn-diode. Geometric variations allow to make a trade-off between the small Schottky diode forward voltage drop and the low on-resistance of a pn-diode.

1. Introduction

We performed two-dimensional simulations of hybrid Schottky-/pn-diodes [1]. These diodes consist of weakly-doped n-silicon with a highly-doped guard ring of p-Si at the surface (see Fig. 1 for a display of the simulated part of the structure). A metallic contact covers the surface including the pn-junction. The weakly doped material forms a Schottky contact with the metal, and the highly-doped guard ring forms an ohmic contact. Between these regions, the contact characteristic must change smoothly from ohmic to rectifying. The whole structure acts as an integrated – yet interacting – combination of a Schottky diode and a pn-diode.

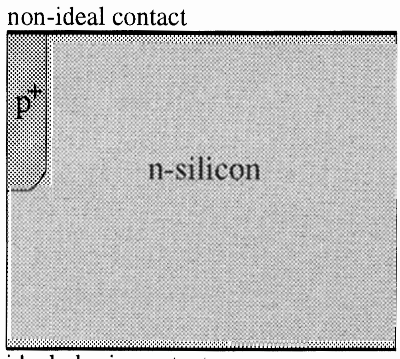

Figure 1: Simulated structure

Because of the varying contact type, this structure cannot be simulated with the conventional models of ohmic and Schottky contacts. Therefore, we used our model of non-ideal metal-semiconductor contacts [2]. The model considers both tunneling and thermionic emission current across the contact and allows the simulation of contacts on very low to very highly doped material with a single model.

We implemented the model into the device simulator PARDESIM [3] as boundary conditions for the Poisson equation and the electron and hole continuity equations. The majority carrier boundary condition models the current density across the contact, consisting of thermionic emission and tunneling currents [2]. The minority carrier boundary condition represents the thermionic emission of minority carriers [2]. The Poisson equation boundary condition is expressed as an apparent lowering of the barrier height, which is due to tunneling [2]. As soon as tunneling occurs through the whole depletion layer, the model switches automatically to the condition of charge neutrality at the contact.

While we reported in [4] on the potential and charge distribution inside the hybrid diode in equilibrium, we investigate in the present paper the electronic behaviour of the device in the forward bias regime.

2. Device simulations

The simulated structure (Fig. 1) is $10\mu m$ wide and $8\mu m$ high, the width of the p^+-region is $1\mu m$. The n-doping is $2 \cdot 10^{15}\mathrm{cm}^{-3}$ and the p^+-doping $10^{20}\mathrm{cm}^{-3}$. On the back-side of the device, an ideal ohmic contact has been assumed.

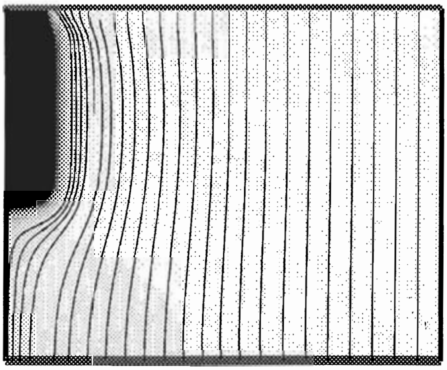

Figure 2: Current pattern at low forward bias

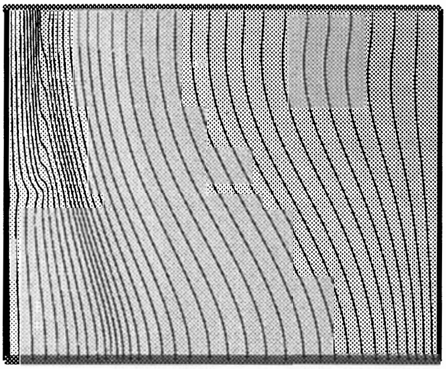

Figure 3: Current pattern at high forward bias

The simulated current distribution under a low forward bias of 0.1 V is shown in Fig. 2 [5]. The results show that in this bias regime the current flows exclusively in the Schottky diode part of the structure. The reason is that the Schottky contact is already in a conducting state, while the forward threshold of the pn-junction has not yet been reached. This situation changes drastically if we increase the bias to 1.5 V. The corresponding flow pattern is depicted in Fig. 3 [5]. Now the pn-junction is in a conducting state, too, and the current flows mainly through the p^+-part of the structure.

Figure 4 shows the simulated I/V characteristics for the forward regime. For small voltages, the Schottky diode part alone is in conduction. At 0.8 V, the pn-junction goes into the conducting state, too, and the current strongly increases. For compari-

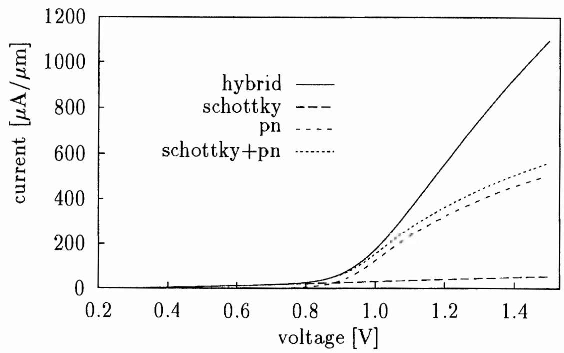

Figure 4: Forward I/V characteristics

son, we included the corresponding curves of a single pn-diode and a single Schottky diode with respective cross-sections, as well as the current of a parallel circuit of these two diodes. We note that the current of the hybrid diode is higher than the current of the equivalent combination of the single pn- and Schottky diodes. This effect is caused by an interaction of the integrated diodes; it has also been observed experimentally [6].

As the simulations show, the effect can be attributed to a reduction of the bulk resistivity by minority carriers injected from the p^+-region. Figure 5 displays the hole distribution in the whole structure. Despite the smallness of the p^+-region, the minority concentration in the whole n-region has increased from the equilibrium value of $7 \cdot 10^4 \mathrm{cm}^{-3}$ to about $2 \cdot 10^{17} \mathrm{cm}^{-3}$, which is even more than the equilibrium *majority* carrier concentration. In order to keep charge neutrality, a strong increase of electrons too is the consequence. This high concentration of free carriers increases the conductivity of the n-region and hence the current in the hybrid device. Since in the equivalent parallel circuit of the single devices an injection of the pn-junction into the Schottky diode cannot occur, the total current in this case is lower.

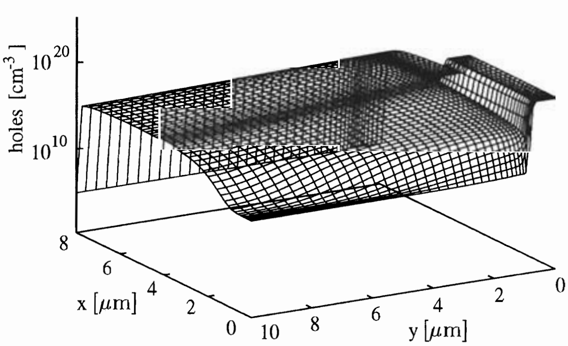

Figure 5: Hole distribution at high forward bias

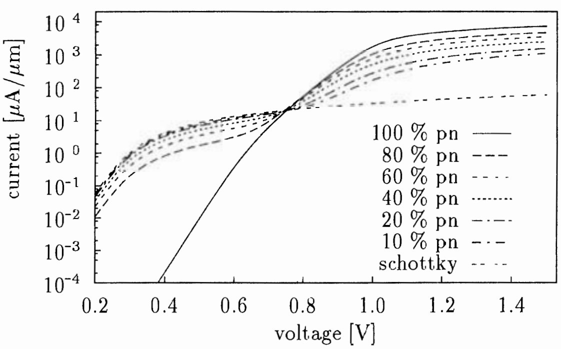

Figure 6: I/V characteristics at various pn/Schottky ratios

3. Investigation of geometric variations

Finally, we investigated the effect of various area ratios between the Schottky- and the pn-fraction. For this purpose, we varied the size of the p^+-region in Fig. 1 from zero to the full width of the structure, thus obtaining a Schottky resp. a pn-diode in the limits, and a number of hybrid diodes inbetween. The resulting current-voltage relationships are shown in Fig. 6.

We observe that the Schottky diode has a low forward voltage drop, but a rather large on-resistance. The pn-diode, in turn, has a high forward voltage drop and a small on-resistance. The hybrid diodes combine these features, thus having a low voltage drop *and* a a small on-resistance for higher voltages. Hence, the area ratio allows to make a trade-off between forward voltage drop and on-resistance. This behaviour also agrees well with the experimental results [6].

In conclusion we note that with the presented simulation model simulation-based optimizations of the device for a specific application become possible.

References

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[5] Picture created with *Picasso* (developed by ETH Zurich and ISE AG, Zurich).

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