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New Spreading Resistance Effect For Sub-0.50 μm MOSFETs: Model and Simulation

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Abstract

A new major spreading resistance (SR) contribution associated with the vertical shift of the peak LDD concentration into the bulk is reported. This contribution is at least a factor of 5 larger than the SR variations of the lateral S/D profile (with peak concentration at the interface) reported so far [1]. The effects are relevant to sub-0.5 μm devices manufactured with reduced thermal budgets. A resistor network model, corroborated by 2D simulations, explains the key features of the effect, including a reversal of SR trends for shallow junctions due to the impact of accumulation resistance (AR). For the first time, ostensibly conflicting data from experiments with various sheet resistances $\varrho_{\square}$, junction depths χ_j, and S/D constructions can now be clearly understood.

1. Introduction

Parasitic S/D spreading resistance is known to be a limiting factor for MOSFET scalability [2]. Baccarani and Sai-Halasz [3] were first to derive an analytical expression for SR assuming an idealized uniform step p-n junction. Subsequently, Seavey [4] has shown that in practical devices Baccarani's first order derivation can underestimate SR effects up to a factor of 5. An authorative study of SR which accounts for the effects of doping gradient including accumulation resistance (AR) is in series with SR has been given by Ng and Lynch [1]. All of these studies, however, are based on the assumption that the peak concentration both of the lateral and vertical S/D profiles is at the interface. This assumption is no longer justified, especially for the S/D extension overlapping the gate electrode. First, because the nature of the lateral profile is not known precisely and is likely to have peak concentration deeper in the bulk; second, because it is advantageous to place the implantation peak somewhat deeper into the substrate to avoid otherwise sheet resistance fluctuations of up to 30% [5]. During the subsequent anneal at a reduced thermal budget the reduced diffusion might not be able to shift the concentration peak back to the interface.

2. The New Spreading Resistance Effects

The impact of concentration peak shifted into the substrate can be explained in terms of a simple resistor network, see Fig.1. The model describes the diffusion sheet resistance $R_{sh} \equiv \varrho_{\square} = 2 \cdot R_{s12} \cdot R_{s22}/(R_{s12} + R_{s22})$ assuming parallel current paths,

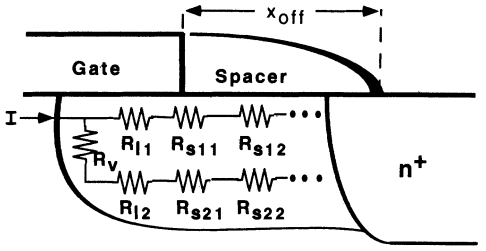

Figure 1: A resistor network describing the spreading resistance in the LDD region. Resistors R_v, R_{l1}, and R_{s11} depend upon gate bias.

and the spreading resistance by $R_{sp} = R_{tot} - R_{sh}$, where $R_{tot} = (R_{l1} + R_{s11} + R_{s12}) \cdot (R_v + R_{l2} + R_{s21} + R_{s22})/((R_{l1} + R_{s11} + R_{s12} + R_v + R_{l2} + R_{s21} + R_{s22})$. R_{tot} contains the components R_{l1} and R_{l2} which describe the increased resistance of the lateral fall-off of the LDD profile. R_v describes the resistor between the parallel resistors in the region of current spreading within the S/D regions. In other words, R_v breaks the symmetry of the resistor network with respect to the current entry from the channel. R_{l1} is the lateral resistor in the gate/drain overlap region and is a function of gate oxide field at the drain.

Of course, more involved networks can be considered, but this 'minimal' model captures the key features of the effects. To illustrate the model consider resistor values given in Table 1 in appropriate units R_o. Three vertical LDD profiles are discussed first: A) peak LDD concentrations at the interface, B) peak concentration in the bulk (close to the junction depth), and C) uniform vertical profile; see the corresponding profiles in Fig.2.

Profile	R_{l1}	R_{s11}	R_{s12}	R_v	R_{l2}	R_{s21}	R_{s22}
A	2	1	1	4	5	4	4
B	5	4	4	4	2	1	1
C	2.92	1.6	1.6	2.92	2.92	1.6	1.6
D	1	1.4	1.4	1.9	2.4	1.9	1.9
E	1	1.5	1.9	1.4	1.7	1.4	1.4

Table 1: Values for resistors, in normalized units, for the model in Fig.1. Cases A, B, C correspond to the profiles in Fig.2 and neglect gate accumulation effects. Cases D and E correspond to 20 and 80 keV implants shown in Fig.5 and include V_G dependence of R_v, R_{l1}, and R_{s11}.

Profile	R_{sh}	R_{tot}	R_{sp}
A	1.6	3.24	1.64
B	1.6	4.95	3.35
C	1.6	3.65	2.05
D	1.6	2.75	1.15
E	1.6	2.42	0.82

Table 2: Sheet resistance $R_{sh} \equiv \varrho_\square$, total resistance R_{tot}, and spreading resistance R_{sp} for resistor inputs from Table 1.

The profiles have been constructed to have identical sheet resistance $\varrho_\square$ and identical junction depth χ_j, with the same construction of lateral profile as an extension (by means of erfc(y), y being the lateral space coordinate) of the vertical LDD profile. The factor of 4 as a maximum variation of concentration values has been chosen for convenience to reflect vertical resistivity variation by one order of magnitude, according to the formula $\varrho = 1.45 \cdot 10^9 (N)^{-0.6}$ [1]. In Table 2 all the above resistances have been calculated for profile A, B, and C. It can be seen that SR for case A (peak concentration at the interface) contributes only 1.64 $R-o$ or 103%(=1.64/1.6) of $\varrho_\square$, whereas in the case B (higher concentration in the bulk) it contributes 3.35 R_o or 209% of the same $\varrho_\square$ - **a twofold increase only due to different geometry (shape) of the network (profile)!** Note that the network is composed from the same resistors; only the parallel resistor rows have been switched. Clearly, SR is a serious

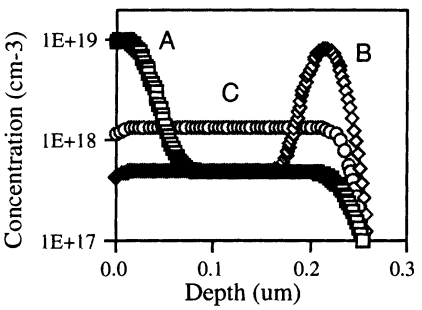

Figure 2: Three extreme cases of LDD profiles with identical sheet resistance and identical junction depth used for MINIMOS simulations of the I-V characteristics in the triode regime.

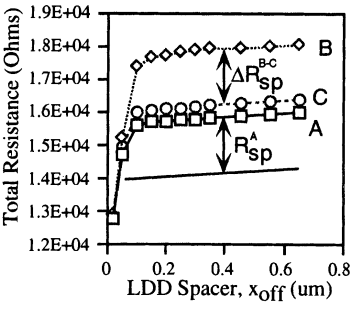

Figure 3: MINIMOS simulations of total MOSFET resistance (V_D = 0.1V, $V + G = V_T +$ 0.2V, $L = 0.5\mu m$, $W = 1.0\mu m$) versus spacer length, x_{off}, for LDD profiles from Fig.2. Beginning at $x_{off} = 0.04\mu m$ LDD regions are completely buried under the n^+ S/D regions.

problem, when the peak concentration is shifted from the interface into the bulk. These trends, however, are reversed for shallow junctions, because of the dominant role of the accumulation resistance in case of very shallow junctions. Accumulation layer is induced in the S/D region by the gate field and extends the inversion layer of the channel into S/D regions. Simulations show that at high enough V_G the LDD accumulation layer underneath the gate in the triode region is almost independent of the original doping levels. In Table 1 resistor values are given for profiles D and E but now, in contrast to profiles A, B, and C, with R_{l1} and R_v now being modified by V_G; R_{l1} has the same value for both profiles D and E. It can be seen from Table 2 that SR for the profile D with peak concentration at the interface is larger than for profile E with concentration peak deeper in the bulk. Profiles D and E from the network model correspond to 20 and 80 keV implants shown in Fig.5.

3. SR Extraction from I-V Characteristics

SR on the source and drain side contribute in different ways to the total resistance. SR on the source side reduces not only the effective drain bias but also the effective gate field which entails higher channel resistance, whereas SR on the drain side reduces only the drain bias. In order to extract the genuine LDD SR, a transistor with n^+ source only and with LDD/n^+ drain has been constructed for various LDD profiles with exactly the same $\varrho_\square$ and χ_j shown in Fig.2. In Fig.3 the **total MOSFET resistance** is plotted for three different LDD vertical profiles, A,B,C, as a function of LDD drain offset x_{off} on the drain side. It can be seen that for large x_{off} all three curves are parallel, reflecting the same $\varrho_\square$, and merge into one point at small x_{off} at which the LDD region begins to be completely buried under the lateral profile of the n^+ region. Obviously, all other quantities being identical, the difference in the curves is due to different SR effects. As expected from the simple resistor model, profile B with a peak in the bulk displays highest SR, and profile A with the peak concentration at the interface has the smallest SR contribution. To compare the effects of lateral profile extensions versus the aforementioned effects, SR is plotted, in Fig.4 for three profiles as a function of various lateral profile extensions. It can be seen that only extreme variations of the lateral profile produce SR effects comparable with effects associated with the shift of the peak concentration into the bulk.

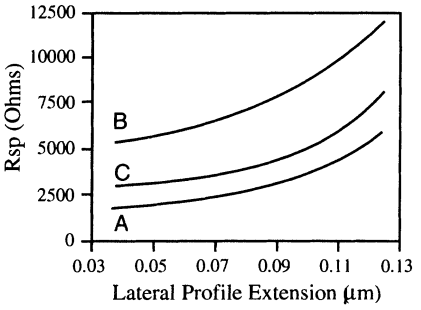

Figure 4: Spreading resistance R_{sp} for profiles A, B, C (Fig.2) as a function of lateral profile extension (slope). In agreement with ref.[1] steep lateral junctions minimize the spreading resistance. However, vertical profile variations are more significant than realistic lateral profile variations.

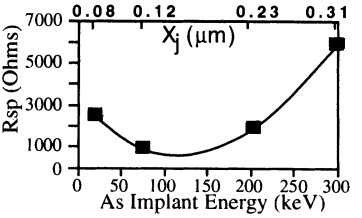

Figure 5: Spreading resistance R_{sp} for As LDD implants as a function of implant energy. (LDD dose adjusted to keep R_{sh} constant.) Reversal effect near $\chi_j = 0.15\mu m$, not predicted by previous models, is clearly seen.

4. Reverse SR Effects For Shallow Junctions

Arsenic LDD regions are investigated with implant energies, $E_{imp} = 20 - 300$ keV corresponding to $\chi_j = 0.08 - 0.32\ \mu m$; the implant doses are adjusted to produce the same $\varrho_\square$. In Fig.5 SR is shown as a function of E_{imp}. It is seen that, in contrast to model predictions [1,3,4], SR is large not only for high E_{imp} but also **low** E_{imp}. The higher SR for very shallow junctions (low E_{imp}) is due to accumulation resistance [1] of LDD region underneath the gate, where profiles with high and low surface concentration display (in the triode region) more or less the same electron concentration. Therefore, profiles with peak shifted into the bulk take advantage of the lower resistance in the bulk, having the same high conductance at the interface by virtue of the accumulation resistance (AR). Hence, reducing the junction depth beyond 0.15 μm with a peak concentration at the interface does no longer reduce the overall SR resistance, but increases it. For deeper junctions SR effects can no longer be offset by AR effects. This happens when the surface concentration region is thicker than the accumulation region. This has important consequences for S/D definition: very shallow χ_j ($\leq 0.1\mu m$) are detrimental not only from $\varrho_\square$ fluctuations, HCI, but also from SR point of view. This study suggests that LDD profiles with concentration peak at 0.04-0.08 μm are optimal. The proposed resistor network including gate field dependent resistor $R_{l1} = R_{ac}$ modeled in ref. [1] provides an excellent basis for SPICE description of parasitic MOSFET resistances.

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