Modeling of Substrate Bias Effect in Bulk and SOI SiGe-channel p-MOSFETs

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Abstract

This paper describes the effect of substrate bias in bulk and SOI SiGe-channel p-MOSFETs. Applying a positive substrate bias to the bulk SiGe p-MOSFETs results in considerable shift of the SiGe channel threshold voltage towards more negative values, and considerable reduction of the saturated SiGe channel hole density, but has negligible effect on the surface channel threshold voltage and hole density. In SOI SiGe p-MOSFETs, the threshold voltages and hole densities are all negligibly affected by the negative substrate bias.

1. Introduction

SiGe-channel p-MOSFETs have generated substantial research work because of higher mobility of holes confined to the SiGe channel[1-6]. In earlier works[4-5], the threshold voltages and hole densities for both the SiGe channel and the surface channel were studied by assuming a zero substrate bias. However, in application circuits, the pass transistors, differential input transistors, and series load/drive transistors in CMOS gates usually have non-zero substrate bias. Thus, this paper addresses the effect of substrate bias on the threshold voltages and hole densities. The bulk n^+ gate SiGe channel modulation doped p-MOSFETs[1], and the SOI SiGe p-MOSFETs[6] will be described.

2. Analysis

2.1 Bulk modulation doped SiGe p-MOSFETs

The bulk modulation doped SiGe p-MOSFETs consists of an n^+ poly gate, a gate oxide of t_{ox}=5nm, an undoped Si cap of t_{cap}=5nm, an undoped graded SiGe channel of t_{sige}=10nm, an undoped Si buffer of t_{buff}=5nm, a modulation doped layer of 4nm with the areal boron density of Q_m, and an n-type substrate of $N_b=5\times10^{16}/cm^3$. Ge is graded linearly from 0.1 at the bottom SiGe/Si interface to 0.3 at the top SiGe/Si interface. Q_m is set to $1.107\times10^{12}/cm^2$ to adjust the SiGe channel threshold voltage at V_b=0V to -0.6V which is usually required by digital circuits. At given gate-to-source bias V_g and substrate-to-source bias V_b, the Poisson's equation in SiGe/Si hetero-structure is solved iteratively[2] by assuming that the quasi-Fermi level of holes is higher than that of electrons by qV_b[7]. In implementation, the simulation depth should increase with increasing substrate bias since the depletion layer becomes wider.

The SiGe channel threshold voltage $V_{t,sige}$ is defined as the gate voltage at which the hole concentration at the top SiGe/Si interface equals the substrate doping. Similarly, the gate voltage at which the hole concentration at the surface equals the substrate doping is defined as the surface channel threshold voltage $V_{t,s}$[4]. Given V_b, $V_{t,sige}$ and $V_{t,s}$ are found using the dichotomizing search.

Fig. 1 shows the simulated SiGe channel and surface channel threshold voltages versus substrate bias. $V_{t,sige}$ increases considerably with increasing V_b from 0 to 3.0V, while $V_{t,s}$ increases slightly. As in Si MOSFETs, the substrate bias enlarges the threshold SiGe/Si interface potential by V_b, thus increasing the bulk charge and the electric field, and hence $V_{t,sige}$. At $V_{t,s}$, because the valence band at the top SiGe/Si interface is pinned at the hole quasi-Fermi level(Fig. 2), and the valence band at the surface is lower than the hole quasi-Fermi level by the following constant difference since the surface hole concentration equals N_b:

$$E_{fp}-E_v(0)=kT\ln\left(\frac{N_v}{N_b}\right) \tag{1}$$

the potential drop across the Si cap can be estimated from the valence band variation as:

$$\phi(t_{cap})-\phi(0)\approx\frac{\Delta E_{v,t}}{q}-\frac{kT}{q}\ln\left(\frac{N_v}{N_b}\right) \tag{2}$$

where N_v is the state density in the valence band, E_{fp} is the hole quasi-Fermi level, and $\Delta E_{v,t}$ is the valence band offset at the top of the SiGe channel. The field across the Si cap according to Eq. (2) is independent of V_b, thus resulting in a nearly constant $V_{t,s}$.

Fig. 3 gives the SiGe channel and surface channel hole densities versus gate voltage at V_b = 0 and 1.0V. The saturated SiGe channel hole density which is a measure of the hole confinement capability is reduced by the substrate bias. This reduction also results from the increased bulk charge, which increases the electric field across the bottom SiGe/Si interface, thus reducing the SiGe channel hole density according to Gauss law. Hole confinement is thus degraded in SiGe p-MOSFETs operating at non-zero substrate bias such as pass transistors or series load transistors in CMOS gates. The saturated SiGe channel hole density versus substrate bias at t_{cap}=5 and 7nm is shown in Fig. 4, where the variation of V_b from 0 to 3.0V reduces the SiGe channel hole density by about $0.8\times10^{12}/cm^2$. The SiGe channel hole density increases markedly with thinning the Si cap at all V_b because of the rise of the field at the top of SiGe channel with $1/t_{cap}$, as in the case of zero V_b[5]. On the other hand, the surface channel hole density curve at V_b = 1.0V almost coincides with that at V_b = 0V(Fig. 3), implying that the surface channel inversion hole density at a given gate voltage is negligibly affected by the substrate bias.

2.2 SOI SiGe p-MOSFETs

The channel cross section of the SOI SiGe p-MOSFETs[6] consists of an n^+ poly gate, a 6.5nm gate oxide, a 7nm undoped Si cap, a 10nm undoped SiGe channel, a 5nm undoped Si buffer, a 150nm $10^{15}/cm^3$ n-type doped silicon film, a 410nm buried oxide, and a silicon substrate with the same doping as the silicon film. The calculation is the

same as that for the bulk devices except that the quasi-Fermi levels for electrons and holes in the silicon film merge with one another and always equal those in the source because of the insulating buried oxide. Another difference is that the substrate-to-source bias in SOI p-MOSFETs is negative instead of being positive in the bulk case since n-channel and p-channel MOSFETs on SOI share the same substrate which is usually grounded[8].

The dependence of $V_{t,sige}$ and $V_{t,s}$ on substrate bias in SOI SiGe p-MOSFETs is given in Fig. 5. Compared to the bulk case, the SiGe channel threshold voltage is much less sensitive to the substrate bias, resulting from the thick buried oxide which causes very weak capacitive coupling between the substrate and the silicon film. For reasons similar to the bulk case, the substrate bias changes the surface channel threshold voltage negligibly. In Fig. 6, the hole densities versus gate voltage at V_b = -5.0 and 0V are plotted. It is worth noting that V_b is usually -5.0V in SOI p-MOSFETs at 5.0V supply[17]. Moving V_b from 0 to -5.0V increases the SiGe channel hole density due to increased control over the depletion charge by the substrate(back gate) which can reduce the electric field across the bottom SiGe/Si hetero-interface. The SiGe channel hole density thus increases according to the Gauss law. The increase, however, is little because of very small buried oxide capacitance. On the other hand, there is no observable difference in the surface channel hole density curve between the two substrate biases. The modeled SiGe channel hole density increases with thinning the Si cap independent of the substrate bias, as in the bulk case.

3. Conclusion

In summary, the positive substrate bias applied to the bulk devices considerably increases the SiGe channel threshold voltage and reduces SiGe channel hole density, while has little effect on the surface channel threshold voltage and hole density. In the SOI case, the threshold voltages and hole densities all show little dependence on the negative substrate bias. The SiGe channel hole density increases with thinning the Si cap independent of the substrate bias in both bulk and SOI devices.

References

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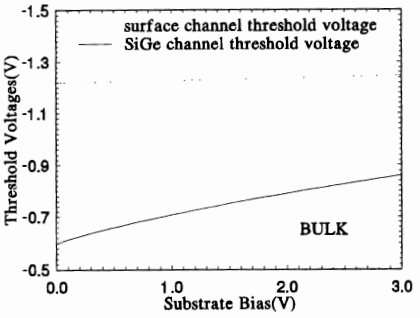

Fig. 1 Threshold voltages versus substrate bias in bulk SiGe p-MOSFETs.

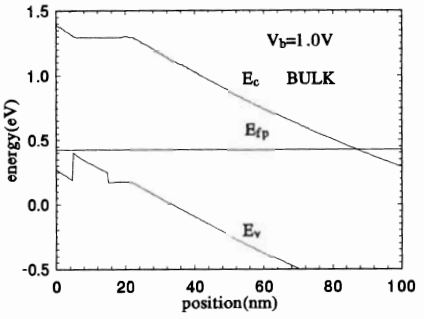

Fig. 2 Band diagram at $V_b = 1.0V$.

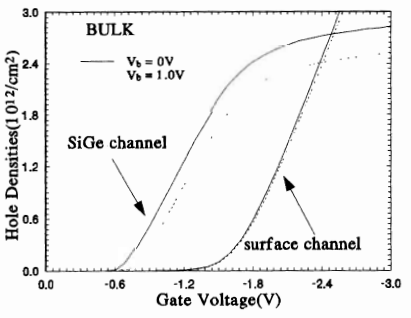

Fig. 3 Hole densities versus gate voltage at different substrate biases in bulk device.

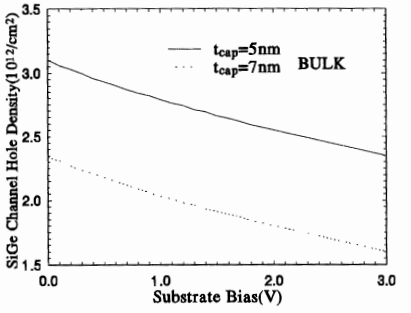

Fig. 4 Saturated SiGe channel hole density versus substrate bias for different Si cap in bulk device.

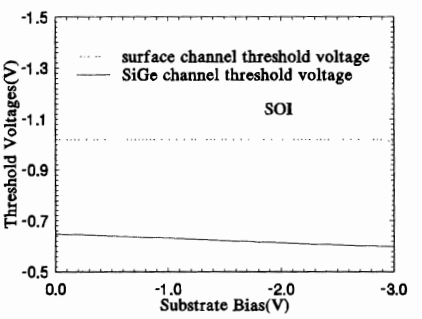

Fig. 5 Threshold voltages versus substrate bias in SOI SiGe p-MOSFETs.

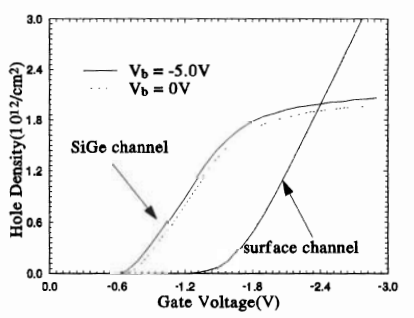

Fig. 6 Hole densities versus gate voltage at different substrate bias in SOI device.