Simulation of Complex Planar Edge Termination Structures for Vertical IGBTs by Solving the Complete Semiconductor Device Equations

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Abstract

In this paper calculations of blocking characteristics for edge termination structures of 600V- and 1200V-IGBTs by means of the device-simulator ToSCA are presented. Because of the efficient grid concept and the properties of ToSCA it becomes possible to solve the complete device equations for very complex grids in relatively short time.

1. Introduction

For the extension of a medium-voltage $1.5\mu m$-MOS-process to higher voltages ($1200V$ up to $2000V$), IC-compatible edge termination structures had to be developed. The shallow pn-junctions ($3...6\mu m$) and the small total passivation layer thickness of 2.5 μm of the process makes a design of an efficient edge structure more sophisticated. But so-called OFP-FLR-structures (Offset Field Plate - Field Limiting Rings) are realizable in spite of the restrictions of the used process. For breakdown voltages up to $2000V$ a lot of field rings are necessary resulting in large and complex structures combined with small sub-elements. In the past amongst analytical methods, mainly field calculation programs solving only Poisson's equation (Depletion model) were used for the simulation of such complex edge structures [1],[2]. These tools are in most cases non-professional, a continuous support and extension of features is only restrictedly possible. Furthermore an including of the mobile carriers to detect for example channel forming or for transient calculations, is very advantageous. So it would be desirable to be able to apply the available professional and semiprofessional device simulators [3],[4],[5], to solve the complete semiconductor device equations. For the following reasons a calculation of complex edge termination structures with these tools is made more difficult:

1. the implemented mesh generators/-editors do not allow a discretization with the necessary resolution and an acceptable number of nodes

2. altogether too little number of nodes

3. convergence problems (especially if floating plates are included) and very long calculation time.

In the paper, calculations of planar edge structures by means of the device simulator ToSCA [5] and further tools of the simulation system PRODESI [6],[7],[8] are presented, for which the problems mentioned above were solved or partly overcome.

2. Mesh generation and mesh editing methods

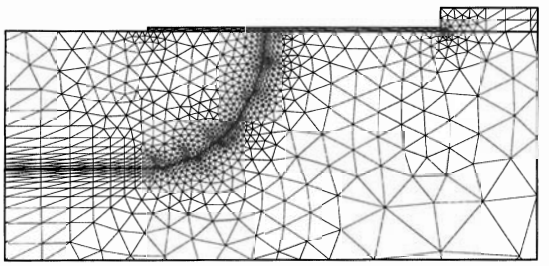

Figure 1: Grid detail of an edge structure

The triangulation was carried out with a novel mesh generator/-editor named TRIGEN [7] and TRIMAN [8], which generates automatically the complete mesh using a global description of the device. This description contains the geometry in terms of polygon curves, the doping profile, the boundary conditions and control parameters. First of all the program tries to adsorb anisotropic triangles at suitable edges or curves located in any direction. So inversion channels, pn-junctions and thin layers can be discretized with a small number of nodes. Remaining regions are covered with isotropic triangles. In Fig. 1 a detail of a termination structure illustrating the grid concept is shown. These mixed isotropic/anisotropic meshes are changeable afterwards in a wide range with the mesh editor TRIMAN. Besides the advantageous properties of isotropic and anisotropic subregions are maintained after all refinement procedures. Because of the connection of isotropic and anisotropic sub-meshes an optimum resolution with an acceptable number of nodes is reached. The numerical properties of the grids are not deteriorated by the anisotropic triangles. Compared to commonly used grid concepts the node saving varied from 1.5...4 depending on the structure, respectively. For the device in Fig. 2 ($1200V$ edge structure) the number of nodes would increase by a factor of 2.1 if an isotropic triangulation is performed.

3. Simulation of the electrical behaviour with ToSCA

The electrical simulation was realized by solving the complete equations of the drift-diffusion model. Additionally to the common mobility, lifetime and intrinsic conduction models the avalanche generation and the different recombination models are included in the simulation. Even with very large meshes (30.000-40.000 triangles) a calculation is possible on workstation with a medium performance in acceptable time. This is attained by the following features of ToSCA, accessory to the efficient grid concept:

1. In ToSCA the complete memory-extensive Newton Jacobian matrix is never used. The coupled equation system is solved successively by a block iteration procedure derived from Gummel's method. So considerably less memory is needed than in comparable simulators.

2. The calculation of the contact currents is done by using the Gaussian theorem and a test function. Because of this very stable contact currents and an accurate current sum are reached resulting in fast convergence behaviour.

3. Due to an automatic switching between the Newton's and Gummel's method the advantages of both methods are combined resulting in a short calculation time. Steps from 20 up to $40V$ are possible without any problems. The switching thresholds are adjustable by the user to an optimal adaption of the problem. In case of involving surfaces states for example a stress of Newton's method results in a reduced calculation time.

4. ToSCA is available in source code completely. So the maximum number of nodes/triangles can be defined by two global parameters before compiling the program. There is no limit for these parameters, so the maximum node number depends theoretically only on the memory of the workstation.

On an Alpha AXP workstation (DEC 3000/300X) with 64 MB memory devices up to 35.000 triangles were calculated with a calculation time of 30 minutes up to 6 hours and breakdown voltages ranging from 600 to $1800V$.

4. Presentation of the simulated examples

In Fig. 2 an OFP-FLR-edge structure for $1200V$-IGBTs with nine non-equidistant steps and a breakdown-voltage of $1510V$ is shown. For three versions of this edge structure the blocking capability was calculated in pseudo-3D-case by using cylindrical polar coordinates. Thereby the blocking capability of the chip corners can be calculated accurately because of their circular shape. In Fig. 3 the normalized

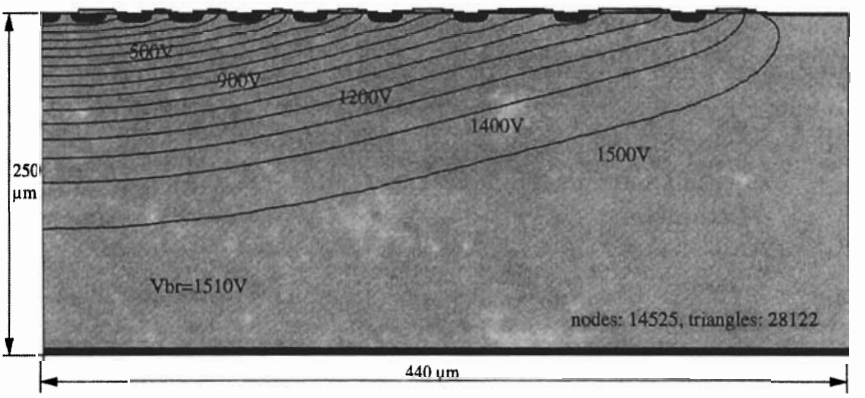

Figure 2: 1200V-OFP-FLR edge structure with non-equilateral ring-spacing

breakdown-voltages is shown for three examples with regard to their breakdown-voltages in ideal two-dimensional case. These three versions differ in the arrangement and the penetration depths of the field rings. As visible in Fig. 3 an inner radius of 150...200 microns is necessary to prevent a considerable decrease of the

blocking capability in the corners. With an increase of the penetration of the field rings the breakdown-voltage goes slightly better, demonstrated by version 1 and 2.

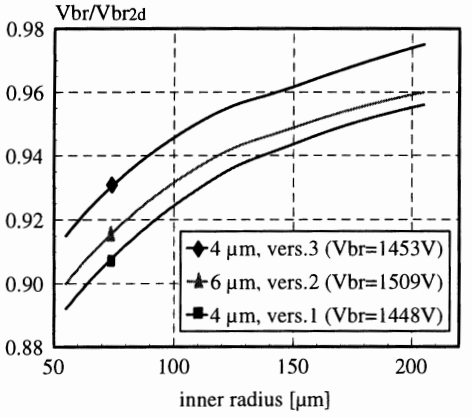

Figure 3: Blocking capability of the corners

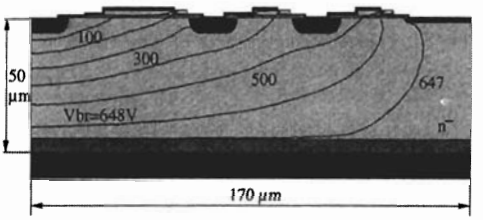

Figure 4: 600V-OFP-FLR-edge termination

But by means of an optimization of the edge structure the blocking capability of the chip corner is noticably improvable (version 3). Fig. 4 contains a $600V$-OFP-FLR edge termination structure for 600V-PT-IGBTs. Because of the less number of steps the mesh generation is distinctly easier compared to the nine-step $1200V$- edge termination. Accordingly only 6.000 triangles are sufficient to triangulate the device with a high resultion. The pn-junctions of all presented examples are dissolved with a value of $250nm$ on the field rings, on the backside emitter with $100nm$. In the substrate of the edge structures there are triangle edges up to $10\mu m$. For the triangulation of very thin layers it was taken care of the fact that all triangles have to evince at least one point inside the layer. That leads to a minimum triangle edge length lower than $50nm$ for example in the gate oxide. The required meshes for the simulation with cylindrical polar coordinates are produced by shifting the x-coordinates of all nodes or by stretching/compressing details of the complete mesh starting from a basic grid.

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