Layout Design Rule Generation with TCAD Tools for Manufacturing

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Abstract

This paper presents a methodology for estimating the effects of changes in the layout design rules on the manufacturability of a VLSI technology. 2-D process and device simulations were used to estimate parametric yield, while functional yield was predicted with state-of-the-art yield modeling tools. A spectrum of TCAD tools was therefore capable of estimating the resulting number of good chips per wafer for different sets of VLSI layout design rules.

1. Introduction

Minimizing the circuit layout feature sizes can lead to improved performance and packing density, but it may also reduce the manufacturing yield. The smaller dimensions increase the relative variability of the process and make the circuits sensitive to smaller particles, which can degrade the manufacturing yield. If that possible reduction in yield is not taken into account properly, it may negate the gains due to greater packing densities.

Layout design rules, at present, are developed by taking the minimum feature size that guarantees process repeatability and no electrical parasitics, while allowing for the tolerance of photolithography steps. Functional yield loss due to particles is usually not considered, and considerable R&D resources are often spent on reducing design rules that do not impact final circuit layout size the most. It is common to treat the probability of failure for each design rule independently, which is not always correct. For example, treating the design rules for minimum metal-1 width and minimum metal-1 spacing independently may underestimate the joint probability of failure because they are inversely correlated, i. e., metal-1 bridging shorts are more likely for wider metal-1 lines.

We present a methodology for the development of layout design rules in a more statistically rigorous way, considering their joint probability of failure, and also taking into account functional yield. Our approach uses TCAD simulation tools and parametric and functional yield loss estimation techniques, and is intended to fit within an integrated process synthesis system [1].

2. Methodology

Figure 1 shows the proposed methodology. Given a process flow and an initial set of design rules,

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the effects of different sets of design rules on manufacturability and electrical were analyzed.

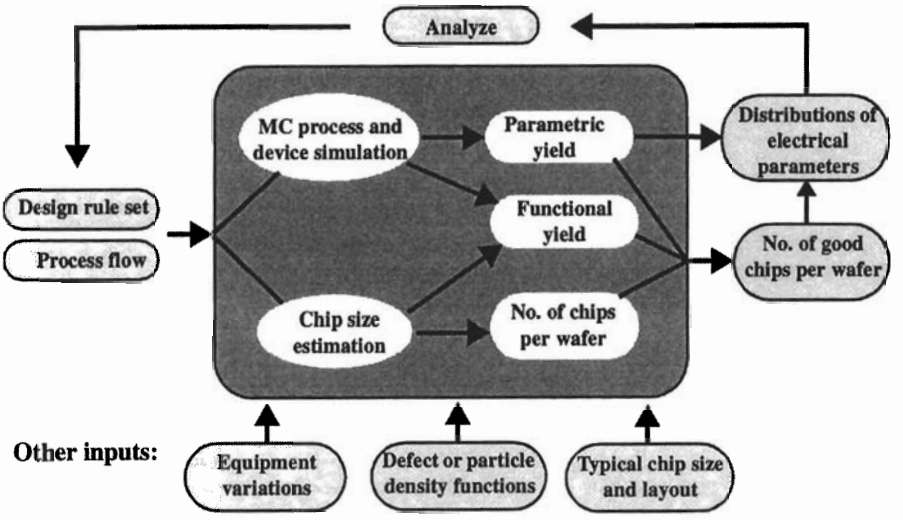

Figure 1: Proposed methodology for design rule development

The process flow for the technology was assumed to be fixed. It was also assumed that it was possible to obtain precise information about the variability of the processing equipment, and measured distribution functions for the density and size of particles or defects. The optimum design rules might be different for different types of circuits (ASICs, DRAMs, etc.,), so the layout of a typical circuit, of the type that the technology was intended for, was used in the analysis.

The measure for performance was the simulated distribution of device characteristics. The metric for manufacturability was the estimation of the number of good chips per wafer for a typical circuit, even though more elaborate cost measurements might be used [2].

2.1. Chip Size Estimation and Number of Printed Chips per Wafer

We have implemented a C program to estimate the impact of the different layout design rules on the size of a typical chip. This program allowed us to approximate the change in size for a small chip or for a typical cell, without having to determine the new layout that the change in design rules required. It would not have been computationally viable to attempt that with a layout compactor.

The approach consisted in decoupling the two-dimensional problem into two one-dimensional ones. The program considered many horizontal and vertical slices, and for every design rule instance in those slices, it decided whether a local shrink or expansion would have been needed to accommodate the new design rules, without calculating the actual changes in the layout features. The total accumulated shrinks or expansions for each slice were then studied and a final change was determined for both horizontal and vertical dimensions. The estimation of the number of printable chips per wafer was then straightforward.

2.2. Monte Carlo Process and Device Simulations and Parametric Yield.

Parametric yield estimation was obtained by introducing equipment variations into the process flow for the 2-D process simulations. The resulting Monte Carlo simulation produced a distribution of electrical device characteristics, instead of single values. Those distributions, with a

set of specification limits, gave the estimated parametric yield [3]. In every case, the electrical parameters were simulated under worst-case operating conditions. Figure 2 shows how the yield loss was calculated, by identifying those points that did not meet the specifications for any of the electrical parameter simulations. Scatter-plots like these only show the interactions between two electrical parameters, while in reality many more parameters were considered.

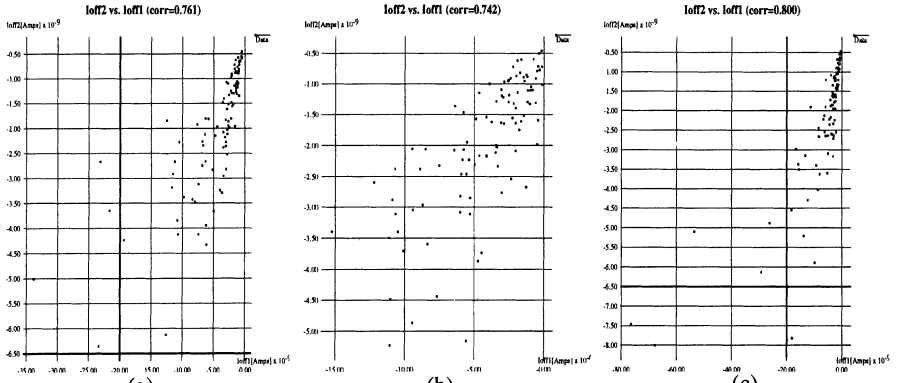

Figure 2: Estimation of parametric yield from simulations, for three changes in design rules: (a) nominal case, (b) reduction in channel length, and (c) reduction in drain spacing. The Ioff for PMOS transistors and the leakage current between two P+ drains are plotted.

2.3. Functional Yield

Functional yield was estimated by integrating the product of the layout critical area function and the defect size distribution function [4]. The critical area for the circuit under study was calculated with the CREST program [5]. If particle size distributions functions were available (form laser-scan and digital image processing equipments), instead of defect size distribution functions, there would be a need to translate the particle size to final defect size -if defects are created at all. That transformation is possible with precise lithography/topography simulators, such as METROPOLE [6]. Finally, the changes in the critical area function due to changes in design rules were calculated by simple shifts in the defect-radius-axis.

3. Application to a CMOS Process

This methodology was applied to a modified 0.8 micron CMOS technology taken from industry. Since we decided to generate design rules for logic circuits, we used a typical cell for those circuits: a 2500 transistor 8-bit multiplier, to study the changes in chip size and the critical area functions. We extrapolated the results to a 500K transistor circuit by multiplying the area by 200.

The effects on electrical performance were estimated using 2-D process and device simulations. We used TMA SUPREM-IV [7] for the process simulations, and SIMOS, a 2-D device simulator within PDFAB [8]. PDFAB, an environment for statistical process, device and circuit simulations, controlled the Monte Carlo runs, linked the different simulators, and extracted the final electrical characteristics.

Table 1 shows the results for the manufacturing aspects of the problem. The metric chosen was the number of good chips per wafer, which, for a fixed process flow, can directly be translated into circuit cost. The effects of three changes in three different design rules were analyzed. In reality, of course, many more rules would have to be considered, and the process flow could also be modified to accommodate the new rules. We were just trying to show instances of situations where

not considering functional yield or interactions could produce very negative results. In this case, only the reduction in drain spacing could be justified from the manufacturing point of view. The increase in packing density for metal spacing reduction did not compensate the associated yield degradation due to larger sensitivity to smaller particles. The defect distribution data came from actual measurements [4]. Finally, the shrinking of the transistor channel length did result in faster devices, but the reduction in parametric yield (due to PMOS transistor leakage) was unacceptable.

Table 1: Results Summary	**Nominal case**	**1 λ reduction in drain spacing**	**1 λ reduction in metal spacing**	**.5 λ reduction in transistor length**
Parametric yield	94%	92%	94%	9%
Functional yield	86.6%	86.6%	78%	86.6%
Total yield:	81.4%	79.7%	73.3%	7.8%
Chip size (as% of initial size):	100%	97.4%	95.4%	96.5%
Number of chips per wafer	200	205	210	207
Good chips per wafer:	**162.8**	**163.4**	**153.9**	**16.1**

4. Conclusions

Functional yield loss due to particles must be considered for layout design rule development: while it might be technologically possible to shrink a technology, it might not be advisable in certain instances, because it would end up producing fewer good chips per wafer. The interactions between different design rules must also be taken into account by studying the joint probability of failure. 2-D TCAD simulation tools and the most advanced yield estimation techniques can be used to study the manufacturability of different sets of layout design rules, by estimating the number of resulting good chips per wafer. The use of TCAD tools could offer significant development cost savings, and help focus R&D investments into the most profitable areas.

5. Acknowledgments

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