Process- and Devicesimulation of Very High Speed Vertical MOS Transistors

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Abstract

Optical lithography does not allow the scaling of MOS transistors down to 100nm dimensions. Thus the channel length of high speed MOS devices must depend on alternative processing steps. In this work layer deposition and etching are analysed with respect to the formation of very short MOS transistors with vertical orientation. Dopant diffusion with very steep gradients are studied in epitaxial layers. Process and device engineering aspects for a vertical MOS transistor at the sidewall of an etched trench are discussed.

1. Introduction

To improve the performance of MOS transistors the structure size of the devices must be scaled down. However the decrease of the channel length below the quarter-micron dimension down to 100nm is limited by optical lithography. To realize very high speed MOS devices within a 500nm lithography environment, alternative approaches are required, in which the channel length does not depend on lithography. Layer deposition and etching allow fine adjustment on the nanometer scale. In addition, during the deposition of epitaxial layers doping profiles with very steep gradients can be performed. Etching and deposition, however, cause vertical structure modifications. Thus the MOS device must also include a vertical orientation [1]. In this work two aspects are analysed:

1. Channel length definition by **epilayer formation** (Fig.1): The layer formation with Chemical Vapor Deposition (CVD) or Molecular Beam Epitaxy (MBE) allows mimimum channel lengths in the sub 100nm region. In the process flow layer deposition with simultaneous doping formation must be followed by thermal oxidation for gate oxide growth. Depending on dopant species and on concentration regime anneals are necessary for dopant activation. We analysed whether silicon bulk diffusion models available in commercial process simulators can be applied to dopant transport in CVD and MBE layers with extrem dopant gradients [2].

2. Channel length definition by **trench etching** (Fig.2): Silicon etching is less expensive and more useful for production engineering than CVD and MBE. Process- and device simulation was used to develop and optimize a vertical MOS transistor at the sidewall of an etched trench. This was done on the basis of more conventional types of processing steps.

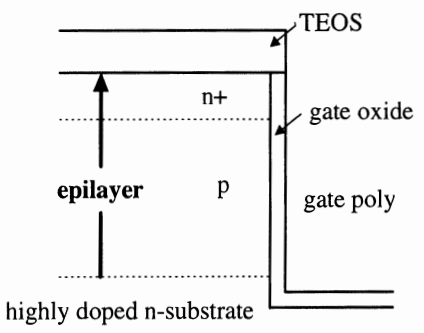

Fig.1: Vertical MOS transistor formed by epitaxial layer deposition.

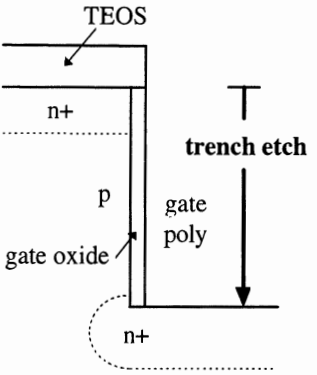

Fig.2: Vertical MOS transistor formed by trench etching and n^+ implantations.

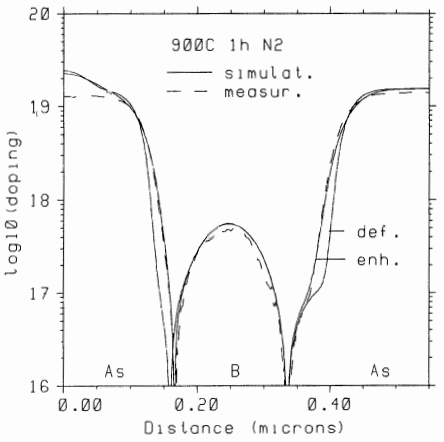

Fig.3: Doping profiles in an annealed CVD epilayer. Default diffusivities for arsenic result in an error of 2*15nm for the resulting channel length.

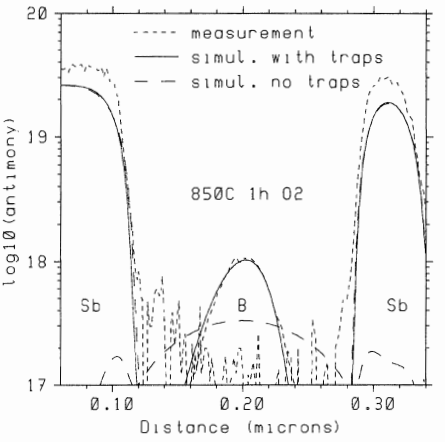

Fig.4: Doping profiles in an annealed MBE epilayer. Boron shows no OED.

2. Dopant diffusion in vertical MOS structures formed by CVD and MBE

The diffusion behaviour of boron and arsenic in CVD layers between 800 and 1000°C in nitrogen atmosphere is investigated. In MBE layers we studied boron and antimony between 700 and 900°C in oxidizing atmosphere. Doping profiles were measured by SIMS. As a result, the silicon bulk diffusion models can be applied to CVD layers by and large. If extrem accuracy is required for sub quarter-micron devices, the diffusivity of arsenic must be enhanced (Fig.3). In MBE layers (Fig.4) antimony diffuses as in silicon bulk. The boron profiles, however, show nearly no oxidation enhanced diffusion (OED) that would be predicted for silicon bulk. Boron diffuses mainly via interstitials which are injected during oxidation. In TEM cross sections the genera-

tion of dislocation loops is observed during thermal treatment. Dislocation loops are known to absorb free interstitials very effectively. Usually the growth and shrinkage of dislocation loops and corresponding capture and emission rates for interstitials cannot be modeled with commercial process simulators. TSUPREM4 [3], however, includes an interstitials trap model. In a first approach this model was used to regard for the capture of interstitials which are generated during oxidation. The total trap concentration was modified to find agreement between the profiles from SIMS and from simulation (equilibrium trap occupation assumed). The total trap concentration increases with temperature suggesting that the size of dislocation loops increases also with temperature. TEM cross sections show no loops before the oxidizing anneal after MBE epitaxy. In summary we conclude that thermal treatment of MBE layers which is necessary for MOS processing creates dislocation loops. These loops affect the dopant diffusion by the capture of interstitials preventing OED.

3. Process and device optimization of vertical MOS structures

In this part we study features in process and device engineering which are important for the formation of a vertical MOS transistor. The channel length is defined by trench etching (Fig.2). The simulations were performed with TSUPREM4 and MEDICI [3]. The doped regions are formed by a trench etch and by implantation. A schematic structure is shown in Fig.2. In contrast to lateral MOS transistors following aspects must be regarded: 1. The vertical profile of implanted arsenic (channeling) forming the upper n^+ region at the silicon surface affects the channel length. 2. A VT-implant is difficult to perform. The threshold voltage must be adjusted by a well. 3. The oxide thickness at the trench sidewall must mask the arsenic implantation (usually tilted) for the lower n^+ region at the trench bottom. 4. Diffusion of the lower n^+ doping around the trench corner is important for the saturation current and device symmetry between between source and drain. 5. If the corners at the trench bottom are rounded (due to isotropic components during trench etching) the saturation current decreases with increasing curvature radius.

The resulting device performance (Fig.5,6) do not differ from conventional lateral MOS transistors.

4. Conclusion

For the development of vertical MOS transistors we have analysed the dopant transport in MBE- and CVD-epilayers during thermal treatment. The results, summarized in the following table,

	boron	arsenic	antimony
CVD, N_2 ambient:	as in Si-bulk	enhanced diffusion	-
MBE, O_2 ambient:	reduced OED (disl.loops)	-	as in Si-bulk

indicate, that epilayers in general cannot be treated in the same way as silicon bulk material. Some authors use MBE layers in experimental structures to determine model parameters for pointdefects [4]. These kind of experiments need an extra analysis, which proofs the quality of the epilayer.

We have also shown that vertical MOS transistors can be fabricated in a production line without expensive processing steps. The channel length of 200nm is far below the limits given by lithography.

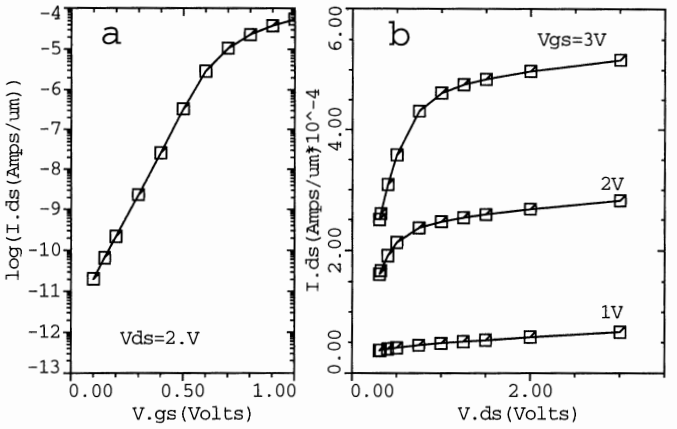

Fig.5: Gate characteristics $I_{ds}(V_{gs})$ (a) and drain characteristics $I_{ds}(V_{ds})$ (b) of a vertical MOS transistor with 200nm channel length (formed as shown in Fig.2.).

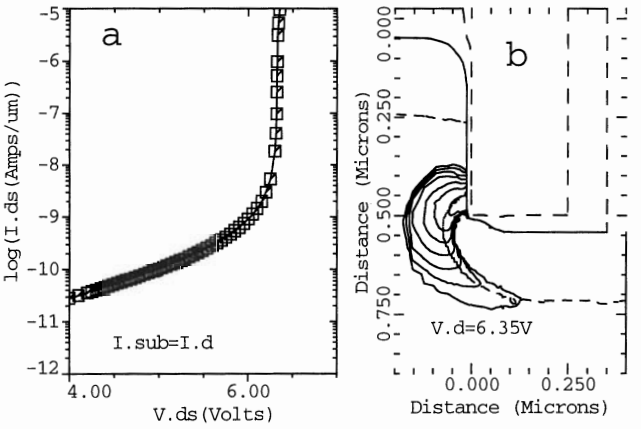

Fig.6: Breakdown characteristics $I_{ds}(V_{ds})$ (a) and contourlines of the impact ionization rate (b) for the same device as shown in Fig.2 and Fig.5.

References

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