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Investigation of GTO Turn-on in an Inverter Circuit at Low Temperatures using 2-D Electrothermal Simulation*

Y. C. Gerstenmaier and E. Baudelot[a]

Corporate Research and Development, Siemens AG
Otto-Hahn-Ring 6, D-81730 Munich, GERMANY
[a]Drives and Standard Products, Siemens AG
G.-Scharowski-Strasse 2, D-91058 Erlangen, GERMANY

Abstract

GTO (gate-turn-off-thyristor) turn-on failure in inverter circuits for traction drives is investigated by mixed-mode 2D electrothermal device and circuit simulation. Whereas GTO turn-off failure has already been analysed extensively in the past, in this paper a novel turn-on failure mechanism at low temperatures is analysed. The turn-on failure is due to a decreased carrier lifetime at low temperature with resulting increased latching current. As a consequence at low load current and low triggering current large parts of the device area do not latch while other parts with somewhat higher carrier lifetime or deviating doping concentration have to sustain a very high current density at high voltages. It is essential for this destruction mechanism to take into consideration the distributed resistance of the gate metallisation and its contact resistance.

1. Introduction

Traction drives at low temperatures (230 - 280 K, i.e. -43$°C - 7°C$) sometimes suffer from sudden GTO-thyristor failure during switching operation. Some evidence points to the occurence of GTO failure during turn-on. This is surprising, because usually in the test circuit turn-off failure occurs but turn-on failure is not observed as long as the admissible dI/dt for the load current is not surpassed.

In this paper a novel GTO turn-on failure mechanism at low temperatures is revealed by 2-D numerical electrothermal simulation. The device simulator [1] solves the complete semiconductor equations (Poisson and continuity equations) together with the heat flow equation for the dynamic development of the lattice temperature within a general external network. Additionally thermal resistors and capacitors can be included in order to allow for the cooling of the device by the packaging.

Fig.1 and fig.2 show the inverter circuit, which is fed by a dc-voltage source. By means of the GTO-switches 1-4 an ac load current is formed with approximate sine waveform (Fig.3). For forming the first positive ac-current half-period, the switches 3 and 4 are not necessary and are therefore omitted in the simulation. Even with this reduction the problem is of severe complexity; so the calculation of only few GTO switching cycles takes considerable CPU-time. Each GTO has attached to it a RCD-protection (snubber) circuit, a freewheeling diode and gate-drive circuit.

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2. GTO failure

GTO turn-*off* failure has already been analysed extensively in the literature [2, 3, 4, 5, 6, 7]. During turn-off essentially two destruction mechanisms have to be dealt with for high power GTOs: current-filamentation during the spike voltage period and dynamic avalanche generation during the tail-phase. On a wafer scale many individual GTO-Segments (> 2000) in parallel contribute to current transport. Due to inhomogenities between different cells in the lateral dopant or carrier lifetime distribution over the device area, current redistribution during turn-off takes place [6] (independently of dynamic avalanche) and may destroy those segments, which carry the most heavy load.

Because of the excessive number of grid-points it is not possible to simulate the whole GTO wafers in the circuit. Therefore a simulation technique [3] is applied, where a homogeneous 4.5kV/3kA GTO (half cell scaled to full wafer size of $36cm^2$ with respect to current) has in parallel a one segment GTO ($0.03cm^2$ area) representing a local perturbation on the wafer by a higher n-emitter doping of 15% and slightly higher carrier lifetime. For simulation the GTO no.2 of fig.1 was substituted by the coupled system of large area homogeneous GTO and small area perturbed segment GTO representing one inhomogeneous GTO (Fig.4).

3. Results and Discussion

Fig.5 shows a simulation result for normal operating temperature of 400 K, where the GTO no.1 is replaced by a closed switch, while the inhomogeneous GTO no.2 is turned on and off every millisecond. The gate triggering unit supplies 20 A for $20\mu s$, 5 A for $5\mu s$ and 2 A for the rest of the on-state period ($300\mu s$). At t=0 the GTO is triggered on and the circuit load current may be adjusted to any value (in our case -10A). I_L rises at a steepness determined by the the ratio of dc-voltage source (2.8 kV) and load inductance (2mH) i.e. with $1.4A/\mu s$.

At the beginning the GTO has a homogeneous temperature of $400°K$. The maximum local temperature after 2ms amounts to $405°K$ and is due to turn-off. The device behaviour is essentially isothermal and no dramatic or dangerous temperature increase occurs.

In fig.6 the starting temperature for the same system is lowered to 280 K. In the simulation a carrier lifetime reduction by a factor 2 compared to 400 K is assumed following the work of [8, 9]. This results in an increased latching current for the GTO under consideration. Therefore, as can be seen from fig.6, the GTO is not fully latched when the gate trigger current reduces to 2A. As a consequence the anode voltage rises to 2kV. On the other hand the perturbed segment of the GTO has a lower latching and triggering current per area than the homogeneous part and has to sustain a high current density at 2kV anode voltage. This leads to a sharp temperature increase in the perturbed segment above the silicon melting point of 1700 K and the device will be destroyed after 0.2 ms, already.

It is essential for this destruction mechanism, to take into consideration the seperate gate-resistors for the homogeneous wafer and the perturbed cell, as indicated in fig.4, which is due to the gate metallisation and contact resistance. The magnitude of the resistors scales inversely proportional to the respective GTO area. Without distributed resistors the gate current of the perturbed cell becomes negative (gate current is extracted from the cell) and adds up to the gate current of the homogeneous GTO part, so that its gate current exceeds 2A considerably. This compensates for

the inhomogenity of the GTO to a large extent, so that in the absence of distributed gate resistors the device will not fail in that period. Once the load current in the circuit has exceeded the latching current of the GTO the GTO will turn on safely. Therefore the failure described occurs only for small load currents.

The simulation results reveal the essential meaning of the latching current for GTO turn-on failure, which has to be smaller than the circuit load current during the gate triggering period.

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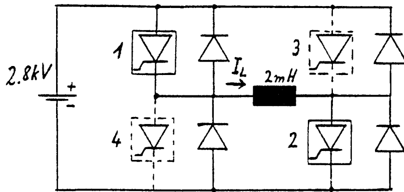

Fig.1: Voltage fed inverter circuit. Each box comprises a GTO-thyristor with snubber and gate circuit as shown in fig.2

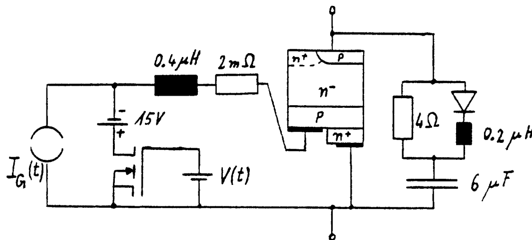

Fig.2: Switch (box) from fig.1, built up from GTO-thyristor with snubber- and gate-circuit. Turn-off is controled by V(t) and turn-on by I_G(t).

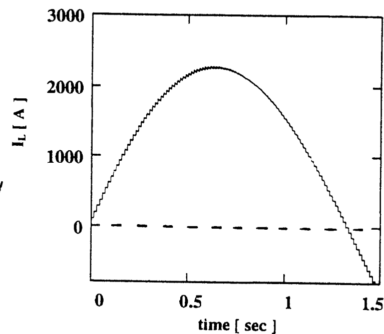

Fig.3: Locomotive-inverter load current at beginning of movement

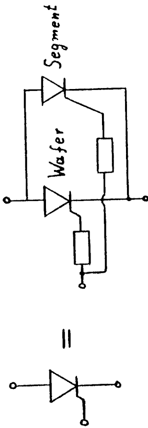

Fig.4: Inhomogeneous GTO, represented for simulation by a homogeneous GTO-wafer (35cm^2 area) and a small perturbed segment with deviating doping and carrier lifetime of 0.03cm^2 area.

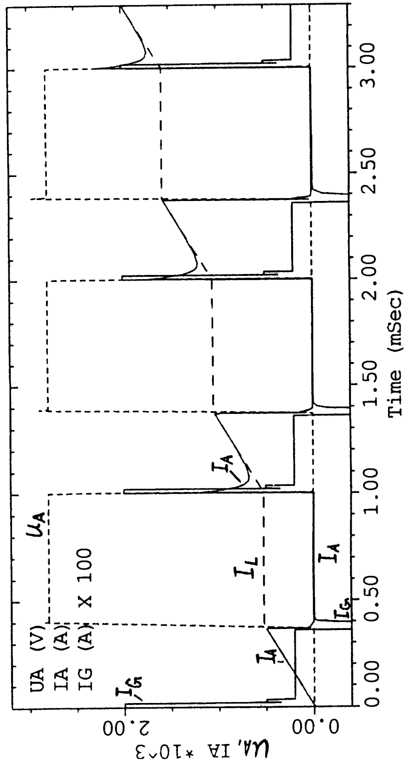

Fig.5: Simulated inverter at 400 K. Dashed line: GTO anode voltage U_A ; solid lines: GTO gate and anode current I_G, I_A ; long dashed line: load current I_L.

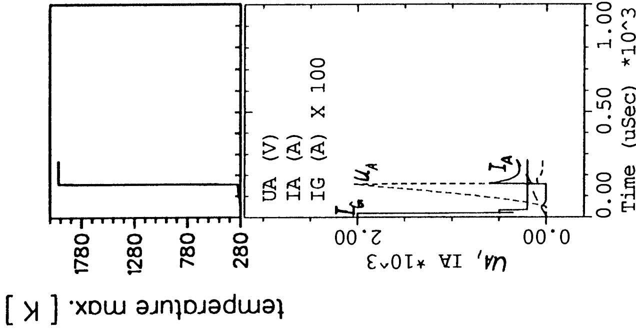

Fig.6: Simulated inverter at 280 K. GTO failure at 0.16ms. Top figure: GTO hot spot temperature.