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An Approach for Explaining Drift Phenomena in GTO Devices Using Numerical Device Simulation

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Abstract

A possible cause for *IGT* drift in GTO thyristors has been identified using numerical 2D device simulation. An increase of the surface recombination velocity under the oxide between the gate and cathode contacts leads to a small degradation of the upper npn transistor gain, which in turn rises the *IGT*. This work focuses on the requirements on the geometrical discretization and on the procedure to extract the DC current gains of the individual transistors that form the GTO thyristor.

1. Introduction

State-of-the-art commercial GTO (gate turn-off) thyristors are subject to a drift of

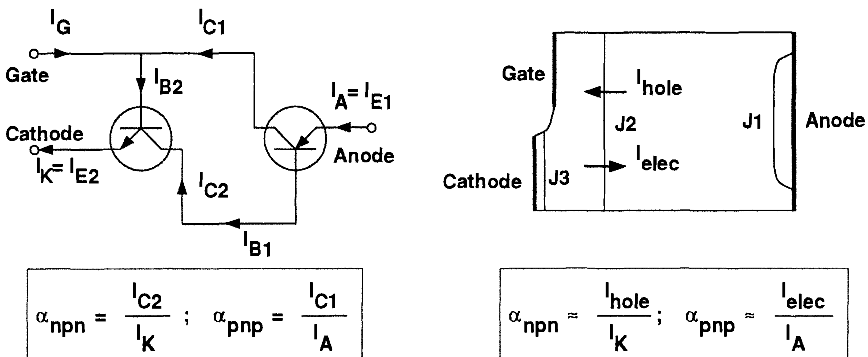

Figure 1: Definition of DC gains

the gate trigger current IGT to higher values, which may even reduce their lifetime as a high power switch. During the operation of a GTO thyristor, the oxide layer between gate and cathode is periodically stressed by high electric fields that occur in its vicinity. There results a degradation of the oxide [1] that reduces the DC gain α_{npn} of the upper transistor in Fig. 1 [2]. The measurement of the DC gains of a GTO device is limited by the following restrictions:

- Only the α_{npn} can be determined
- The measured device must have anode shorts
- The hole injection from the anode side must be close to zero

Using numerical device simulation, these restrictions can be overcome. The electron and hole currents through the center junction J2 can be determined and from that, the individual transistor current gains can be calculated. The gains must be known to determine the trigger point, since at the trigger point the equation holds:

$$\alpha_{npn} + \alpha_{pnp} + I_A \frac{\partial \alpha_{pnp}}{\partial I_A} = 1.$$

2. Requirements on the geometrical discretization

At very small forward biases of the junctions J1 and J3, the forward current density and therefore the gains α_{pnp} and α_{npn} are dominated by recombination processes in the very narrow space charge region. Hence, the grid lines of the geometrical discretization have to be very dense in these areas. Figure 2 shows a comparison of the calculated recombination rates at low current densities of devices with three different grids. The value on the x-axis defines the distance from the junction J3. Grid lines exist at the position of the symbols. The figure clearly shows that the grid lines around the

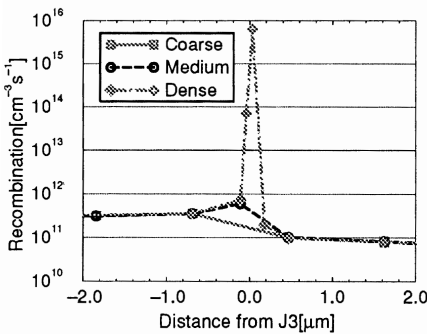

Figure 2: Recombination for different grids

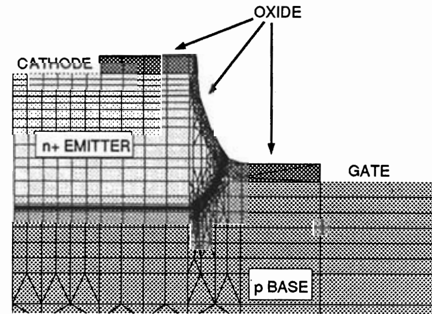

Figure 3: Proper discretization of junction J2

junctions must not be further apart than about $100nm$. Otherwise the recombination is not calculated properly and the derivation of the current gains is not correct. The grid shown in Fig. 3 leads to an accurate calculation of the recombination processes across the junction J3. This grid was generated using MDRAW [3].

3. Derivation of the transistor current gains

In general, it is not possible to measure the transistor current gains in a GTO thyristor since they depend by definition on internal currents. Devices with shorts on the anode side, however, can be regarded as npn transistors as long as the injection from the anode side is negligible. This measurement is restricted to the α_{npn} and to small forward biases. There exist no such restrictions when using numerical device simulation, because it is possible to determine the values of internal currents.

The following procedure was carried out for the determination of the individual current gains:

1. Using the device simulator DESSIS [4], a positive anode bias was applied to the GTO thyristor before the gate current was ramped up to the trigger point. During the ramping of the gate current, contour plot files were saved at regular distances.

2. The electron and hole current densities through the center junction J2 were extracted from the contour plot files and integrated over the width of the device, thus obtaining I_{elec} and I_{hole} (see Fig. 1).

3. The DC current gains were approximated as

$$\alpha_{npn} \approx \frac{I_{elec}}{I_{cathode}}, \quad \alpha_{pnp} \approx \frac{I_{hole}}{I_{anode}}.$$

Making use of a script language, all these steps were carried out automatically. This method is applicable to GTO devices with anode shorts as well as GTO thyristors with homogeneous anode.

Figure 4 shows typical gains as a function of the conduction current densities for a device with a shorted anode (left side) and a homogeneous anode without shorts (right side). While the α_{npn} look alike in both cases, the α_{pnp} are quite different. Due

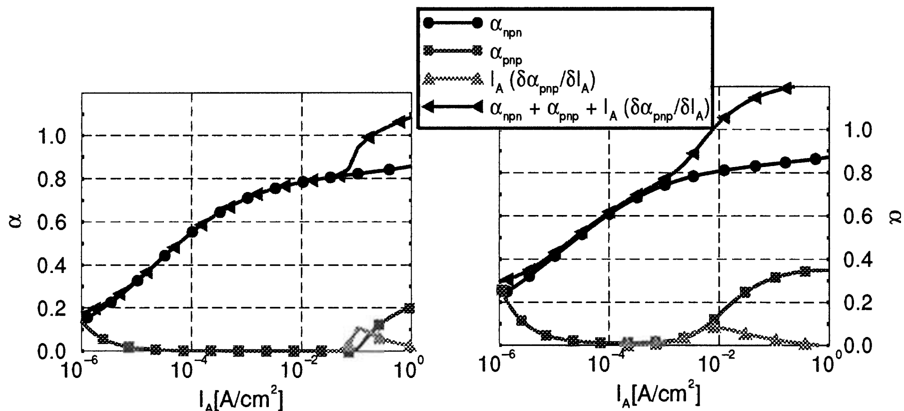

Figure 4: DC gains of shorted (left) and un-shorted (right) GTO during triggering

to its homogeneity, the anode of the device without shorts starts to inject at much smaller current densities and also the trigger point is reached at a smaller current density.

4. Drift simulation results and discussion

The degradation of the oxide layer between gate and cathode, which results from the periodical stress by high electric fields, was modeled in the simulation by varying the recombination velocity at the interface between silicon and oxide (see Fig. 3). The influence on the gain of the npn section of the shorted GTO was then calculated. Furthermore, the impact of the gain variation on the gate trigger current (IGT) and the holding current (IH) was studied. The results are summarized in Tab. 1. The α_{npn} was sampled at an anode current density of $100mA/cm^2$, making sure that the device was not yet triggered.

Table 1: Influence of variations of the surface recombination velocity on DC gain, IGT and IH

Recombination Velocity		$0cm/s$	$2 \cdot 10^3 cm/s$	$5 \cdot 10^3 cm/s$	$1 \cdot 10^4 cm/s$
GTO with anode shorts	α_{npn}	0.822	0.818	0.814	0.807
	$IGT[mA]$	1030	1060	1100	1164
	$IH[A]$	175.1	183.1	187.1	203.1
GTO without anode shorts	α_{npn}	0.740	0.736	0.730	0.722
	$IGT[mA]$	25.8	26.9	28.5	31.2
	$IH[A]$	4.03	4.35	4.41	4.98

Table 1 shows that the degradation of the oxide (increase of the surface recombination velocity from $0cm/s$ to $1 \cdot 10^4 cm/s$) leads only to minor changes in the α_{npn} of less than 3%. The device without anode shorts shows more pronounced changes because of the lower absolute current level. The monotonous decrease of the gain with higher surface recombination velocities can be attributed to the higher recombination current, which adds up to the gate current and therefore lowers the gain.

The impact on the device parameters is much larger than that on the gain. The gate trigger current IGT rises by 13% and by 21% for the shorted and the non-shorted device, respectively. Due to its much lower absolute current level, the relative drift of the non-shorted GTO thyristor is substantially higher than that of the shorted device. Nevertheless, such a GTO is less sensitive in an application, because of its very small absolute value of the IGT drift. The simulated values coincide reasonably well with the increase of the IGT resulting from drift, wich is typically measured during the lifetime of a GTO device. Numerical device simulation thus contributes significantly to the analysis and understanding of reliability issues in modern high power GTO thyristors.

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