HFET Breakdown Study by 2D and Quasi 2D Simulations: Topology Influence

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Abstract

The study of breakdown phenomena is very important for power devices. Indeed, it constitutes a great limitation for the performance. This paper proposes to study this phenomenon by two means: a two dimensional energy model and a quasi two dimensional model. The aim of this work is the optimization of the shape of the gate-recess in order to improve the breakdown voltage, taking into account the microwave performance.

1. Introduction

The breakdown phenomenon is one of the most limitative effect for power devices. The proposed study concerns the influence of specific parameters such as the gate length or the gate-recess configuration, on the breakdown voltage. The corresponding microwave device performance is also investigated for different structures such as conventionnal, or pseudomorphic or δ-doped layer AlGaAs/GaInAs/GaAs HFETs, for power applications.

2. Modeling description

The proposed study is based on two different physical simulation tools:

2.1. The two dimensional hydrodynamic energy model

This model takes into account a large part of the physical phenomenon which occur in HFETs. It is based on a set of equations deduced from Boltzmann's transport equation: continuity, energy and momentum equations combined with Poisson's equation [1]. These equations are solved numerically using a finite difference method with non-uniform meshes and variable time steps. The main advantage of this model is the accuracy of the results, but it needs very large computing time due to a large number of mesh points and the use of small time

steps. Recent improvements have been brought into the simulation i.e. the breakdown phenomenon and the possibility to study real gate recess topologies.

2.2 The quasi-two dimensional model

In this model simplifying assumptions are introduced, but it accounts for the non-stationary electron dynamic effects that are of particular importance for submicron gate devices [2]. The model is based on successive resolutions along the transversal and longitudinal axes. In a first time, the charge control law of the device is computed (transversal axis) and in a second time, the average values of the physical parameters are calculated using the current equation, momentum and energy conservation equations and Poisson's equation (longitudinal axis). The main recent modifications concern the minority carrier consideration and the introduction of a generation term in the equations for hole and electron currents. In order to simplify our calculation, the hole effect is neglected in the charge control law.

Note that the two simulations, associated for the HFET breakdown study, present each their own advantages. The two dimensional model main characteristic is the physical accuracy but it needs large computing time. The validation of the quasi two dimensional model results is made by the physical simulation. Then many different structures and topologies are investigated by the quasi 2D model which needs smaller computing time.

3. Main results

The gate recess offset constitutes the main parameter which makes it possible to improve the breakdown conditions. Its influence is studied on the physical behaviour of the transistor i.e. on the main parameters of the small signal equivalent circuit and on the breakdown voltage. The physical quantities (charge concentration, total energy and potential distributions) are represented in figure 1 for a 50 nm gate recess offset device corresponding to a δ-doped layer HFET structure made by Thomson TCS [3]. A high carrier concentration in the well, a large electric field and energy domain can be remarked at the edge of the recess on the drain side. Figure 2 shows the carrier concentration for a similar device. It can be noticed the carrier injection in the buffer, the charge accumulation in the well and at the exit of the gate, and also the depleted zone under the gate recess. The average energy in the channel is represented figure 3 for a 0.3μm gate length device. The evolutions show that the distance X for energies over 0.7 eV (supposed to be the minimum value for which ionisation phenomenon appears) decreases when the gate recess offset increases. So the breakdown voltage will be improved with wider gate recess offsets as shown in figure 4. The influence of the gate length is shown in figure 5. A decrease of the breakdown voltage is noted for 0.15 μm gate length devices due to a larger average energy in the channel. A more complex topology can also be investigated by the two dimensionnal model, for instance the double recess structure. Figure 6 represents the corresponding total energy distribution. For this device, the energy domain is able to spread along the second recess and as a consequence, a better breakdown voltage will be obtained.

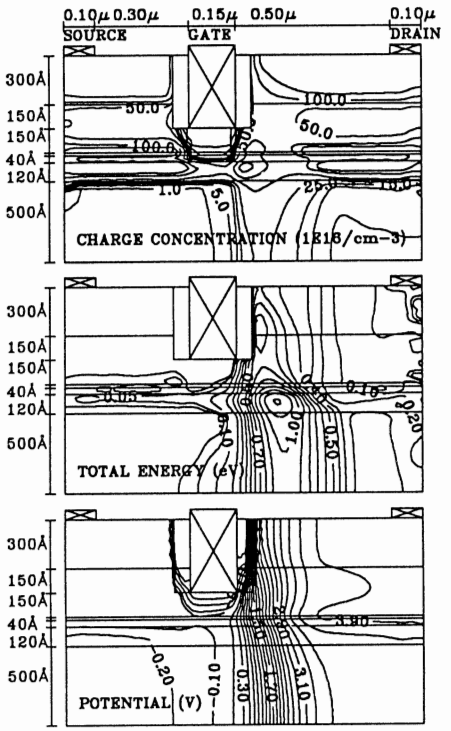

Fig.1 : Charge, energy and potential distributions δ-doped layer HFET
(R = 50 nm, Vds = 4 V, Vgs = 0 V)

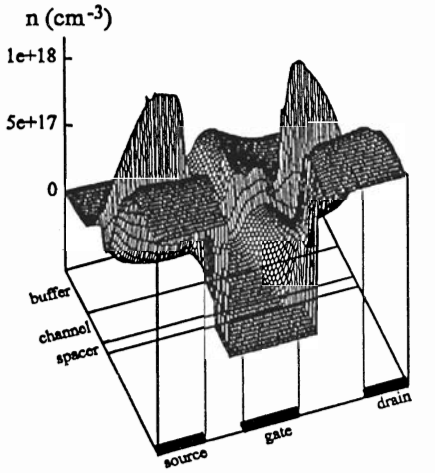

Fig. 2: Distribution of the charge concentration in a gate recess PM-HFET
(R = 100 nm, Vds = 4 V, Vgs = 0 V, Lg = 0.3 μm)

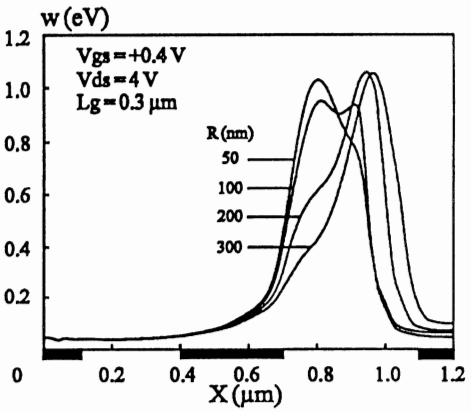

Fig. 3: Evolution of the average total energy in the channel for different gate-recess offsets

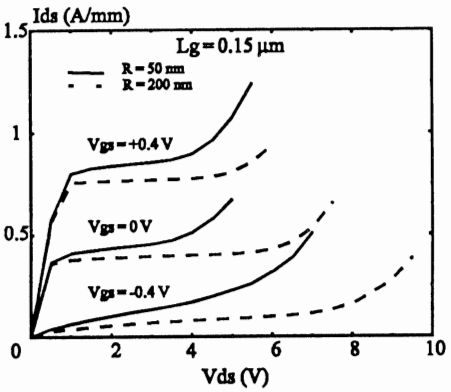

Fig. 4: Current voltage characteristics for two gate recess offsets

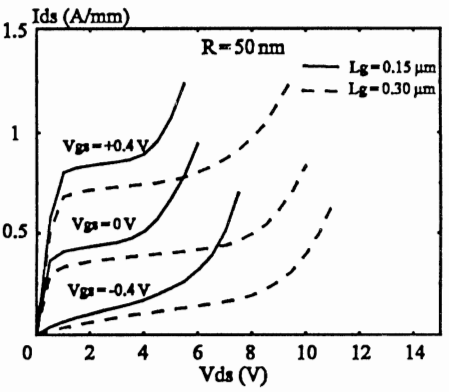

Fig. 5: Current voltage characteristics for two different gate lengths

In order to optimize power devices, the study of microwave performance is also developed by considering structures with larger gate recess offsets. The evolution of the main parameters of the equivalent circuit and the device cut-off frequency are studied for different structures. Figure 7 shows for example the intrinsic current gain cut-off frequency evolutions for two different gate recess offsets. A decrease of f_d is observed for wider gate recess offsets mainly due to a decrease in transconductance.

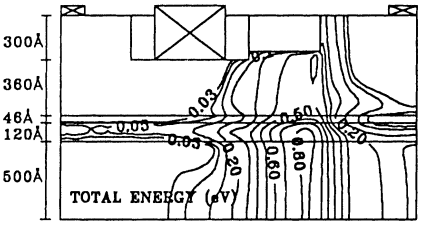

Fig. 6: Energy distribution in a double-recess PM-HFET (R = 100 nm + 300 nm, Vds = 4 V, Vgs = 0 V, Lg = 0.3 µm)

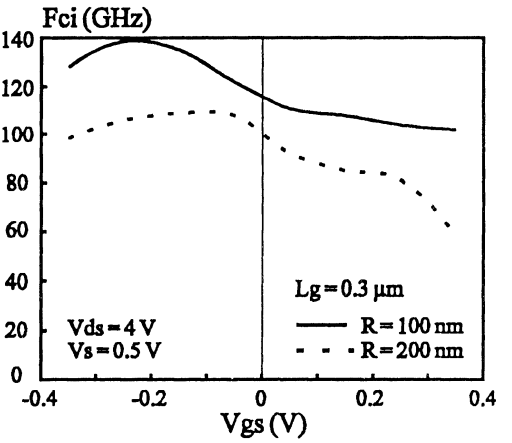

Fig. 7: Influence of the gate recess offset on the intrinsic cut-off frequency

4. Conclusion

This study, obtained by two different simulation tools makes it possible to describe the conditions to respect for power devices optimization. It shows that a compromise between an improvement of the breakdown voltage and the microwave capabilities has to be found. In particular a gate recess offset close to 0.1 µm seems to be the optimum value.

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References

[1] T. Shawki, G. Salmer and O. El Sayed, IEEE Trans. on E.D. Vol. 37, p20-21, n°1, 1990.

[2] H. Happy, G. Dambrine, J. Alamkan, F. Danneville, F. Kaptche-Tagne and A. Cappy.
Int. J. of Micro. and mm-Wave Comp.-Aided Eng. Vol. 3, n° 1, 1993.

[3] 4th Esprit-Classic report, March 1994.