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Performance optimization in Si/SiGe heterostructure FETs

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Abstract

In this paper we investigate the role of structure design in determining high effective mobility (μ_{eff}) values in Si/SiGe FETs. To this purpose we have developed a one-dimensional self-consistent Schrödinger-Poisson simulator and applied it to the study of the mobility behavior of different Si/SiGe FET structures. As a result we propose a structure which, despite to its simple design, shows improved theoretical performance.

1. Introduction

High μ_{eff} is crucial to obtain high-speed, high-performance transistors [1]. Since record high μ_{eff} values in Si/SiGe heterostructures were demonstrated both at low [2, 3] and room temperature [4, 5, 6], the Si/SiGe system is a promising candidate to carry on the improvement of performance standards in modern technologies. However, the strengths of this novel technology for future ULSI still have to be demonstrated.

In Si/SiGe structures the channel quantum well forms inside a Si layer lying on a fully-relaxed SiGe buffer, thus it is subject to tensile strain. The quantization and strain are responsible for the improved mobility with respect to bulk silicon, since they induce an energy splitting between the fourfold degenerate conduction band belonging to the growth plane and the twofold one along the growth direction. Consequently, since electrons inside the twofold band show the lower effective mass to the transport direction and since their quantized levels are lower in energy, the 2D electron gas (2DEG) μ_{eff} is improved. In addition, the spatial separation of the transport layer from the insulator tends to avoid the presence of surface scattering mechanisms limiting electron μ_{eff} .

2. The simulator

To address the problem of the simulation of μ_{eff} in Si/SiGe structures, we have developed a one-dimensional self-consistent Schrödinger-Poisson simulator which fully accounts for the 2D nature of the carrier gas.

First, the simulator computes the strain-induced energy splitting in the frame of the model-solid theory, following [7]. Then, eigenvalues and corresponding envelope functions are determined as result of a self-consistent Newton iteration loop between Schrödinger and non-linear Poisson equations.

From energy eigenvalues and eigenfunctions the scattering rate for the 2DEG are computed. We have included optical, acoustic elastic phonons, and surface roughness to evaluate the impact of surface vicinity. Optical and elastic acoustic phonon scatterings among subbands were included in a conventional way [8]. Surface roughness scattering was implemented as a many-subband generalization of the model described in [9]. The transport parameters we used are those of [10] for phonon scattering and of [11] for surface roughness.

3. Simulation results

As already mentioned, the theoretical peak performance of this technology is very promising, but practical requirements, such as bias compatibility, impose large gate voltage swings that eventually degrade μ_{eff} . In fact, as gate bias is increased, an inversion layer is progressively formed at the surface, thus competing with the channel 2DEG in determining μ_{eff} . In these conditions, a strong limiting effect on μ_{eff} due to surface roughness is expected. In order to fully exploit the possibilities of the material, this effect must be avoided by means of a proper device design, or at least pushed towards higher gate bias.

In the preliminary stage of our work, we applied the simulator to reproduce available experimental data for electron μ_{eff} in real devices [12]. We report here the behavior of μ_{eff} both as a function of temperature (Fig. 1) and of gate bias (Fig. 2) for a structure like the one described in [11], with a 5 nm SiGe cap layer.

In a second step we exploited simple modifications to the structure design in order to improve the confinement of the 2DEG inside the quantum well. The improved structure we propose in this paper is shown in Fig. 3.

Compared to the one in [11], the modulation doping layer has been removed, the n^+-poly has been replaced with the p^+ one, and n doping has been added to the SiGe cap layer and to a small fraction of the SiGe relaxed layer. The presence of the p-poly determines a band bending at the surface of the device that tends to keep the carriers away from the Si-SiO_2 interface, while the n-doped cap layer, as in buried channel MOSFETs, spreads the electrons of the surface channel deeper in the device when the gate voltage is increased, thus displacing the centroid of the electron charge away from surface. Instead, the strained-Si quantum well region was kept intrinsic in order to avoid ionized impurity scattering.

The behavior of the bottom of the conduction band of the new structure as a function of the gate bias is reported in Fig. 4. As in buried channel devices, the n-doped surface layer shows a smooth band bending, thus spreading the electrons of the channel deeper in the device.

For this structure a linear extrapolated threshold voltage of approximately 1 V is obtained (inset of Fig. 4). Although slightly high, this value is positive (as opposed to the negative V_T of the structure of [11]), and can be adjusted by changing the doping dose of the n layers.

As expected, the μ_{eff} behavior as a function of V_{GS} is also improved, as shown in Fig. 5. The peak value (above 2800 cm^2/Vs) is similar to the one reported for the structure of [4, 5] (2600 cm^2/Vs) that we also simulated to check the prediction ability of the simulator.

Finally, as a test on device performance, we report in Fig. 6 the linear transconductance behavior of the new structure. Since we are solving the one-dimensional equilibrium problem, no information on the saturation properties of the electron gas can be directly extracted, as well as 2D effects such as the short channel ones. Nevertheless, the g_m in the linear regime can be estimated. The g_m curve of Fig. 6 has been obtained multiplying the sheet concentration of the inset of Fig. 4 by the mobility curve of Fig. 5, assuming L_{eff} =0.5 μm and V_{DS}=0.2V (corresponding to an average longitudinal electric field of 4 kV/cm).

4. Conclusions

We have investigated the role of structure design in determining high μ_{eff} values in Si/SiGe FETs. A one-dimensional self-consistent Schrödinger-Poisson simulator has been developed and applied to the study of the mobility behavior of different Si/SiGe FET structures. As a result, we have proposed a relatively simple structure design showing improved theoretical performance.

5. Acknowledgments

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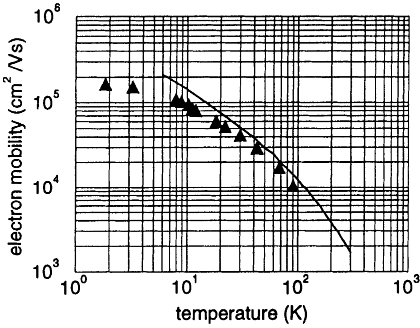

Fig. 1 Zero field electron mobility versus temperature for the 5 nm cap layer device of Ref. [11]. Triangles: experimental Hall mobility data from [12].

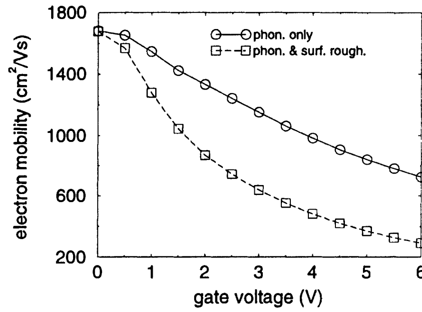

Fig. 2 Zero field electron mobility for the 5 nm cap layer device of Ref. [11].

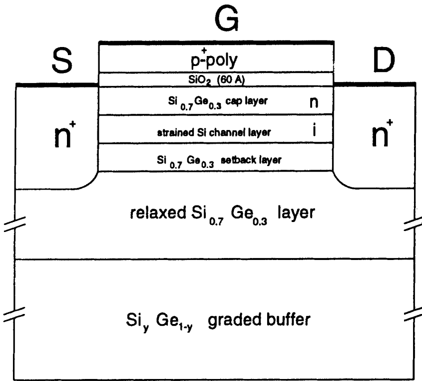

Fig. 3 The proposed structure. The channel resides inside the strained intrinsic silicon layer.

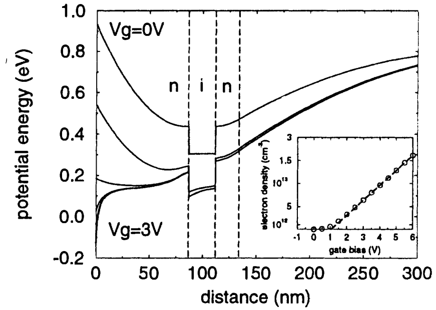

Fig. 4 Self-consistent potential energy profile at different gate voltage of the simulated structure. The voltage step is 0.5V. Inset: integrated sheet charge versus gate voltage and extrapolated threshold voltage.

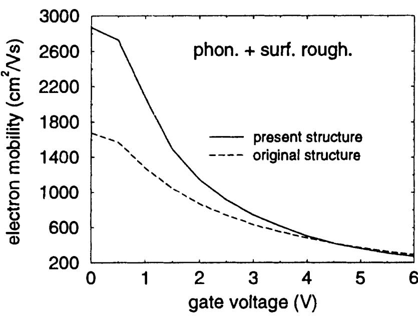

Fig. 5 Zero-field effective electron mobility as a function of the gate voltage for the proposed (solid) and original (dashed) structures.

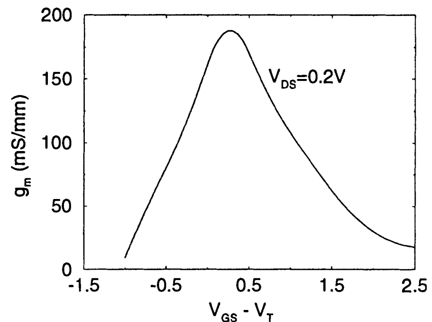

Fig. 6 Linear transconductance versus gate voltage for the proposed structure assuming L_{eff} =0.5 μm and V_{DS}=0.2 V.