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Lifetime Calculations of MOSFET's Using Depth-Dependent Non-Local Impact Ionization

M. J. van Dort, J. W. Slotboom, G. Streutker, and P. H. Woerlee

Philips Research Laboratories
P.O.Box 80.000, NL-5600 JA Eindhoven, THE NETHERLANDS

Abstract

In this paper, we present a simple but accurate engineering tool for optimizing the lifetime of MOSFET's against hot carrier degradation. The method consists of simulation of the substrate currents in conjunction with the use of an empirical relation between the transistor lifetime and the MOSFET currents. Accurate calculations of the substrate currents are only possible if depth-dependent impact ionization is used in combination with the energy-balance equation.

1. Introduction

Hot carrier degradation of MOSFET's has been investigated extensively. Experiments have shown the existence of empirical relationships between the lifetime against hot-carrier degradation and the currents in a MOSFET. For n-channel MOSFET's at the worst-case bias conditions, the lifetime is simply determined by the ratio of the substrate and the drain currents [1, 2, 3, 4]. This relationship is of course technology dependent, but does not depend on the process generation. The simplest way to predict the lifetime of an n-channel MOSFET is to combine the calculated currents with the empirical relation for the lifetime. The accuracy of the resultant lifetime is then determined by the accuracy of the simulation of the drain and substrate currents.

We have tested the method on a set of devices belonging to different fully-optimised process generations (from 2.0 down to 0.17 μm). The leveling-off of the maximum allowable power supply voltage with decreasing design rule is correctly simulated.

2. Substrate currents

It is of course possible to tune the impact-ionization coefficents to match the calculated with the measured substrate currents of a certain MOS generation, but if we want accurate results for the substrate currents over a wide range of MOS generations with a single model, two physical mechanisms have to be taken into account. Firstly, the mean free path of an electron near the Si-SiO_2 interface is significantly smaller than in the bulk of the substrate, and impact ionization in this region is therefore not as efficient as far away from the interface. Impact ionization near the Si-SiO_2 interface was experimentally investigated in surface CCD, where the currents flow very close

to the interface (Fig. 1, [5]). In an MOS transistor, the position of the maximum generation rate depends on the bias conditions, but is generally close to the interface. Secondly, for deep-submicron MOSFET's the lateral electric field peaks are very steep and narrow, and due to non-local effects the carriers are not very efficiently heated up. For a realistic treatment of the substrate currents, we therefore have to introduce a depth-dependent impact ionization model for non-local carrier heating.

For the modeling of the high-energy tail of the electron distribution, we have used the model proposed in [6]. In Ref. [6], it was shown that the solution of the energy-balance equation calculated in post processing is sufficiently accurate to account for the non-local effects of the carrier heating in advanced MOSFET's and in bipolar transistors.

After the determination of the electron temperature T_e, the impact ionization rate is calculated using the bulk [7] and the surface [5] ionization parameters to obtain $\alpha_B(x, y)$ and $\alpha_S(x, y)$, respectively. The effective impact ionization rate α_{eff} is then approximated by

$$\alpha_{eff}(T_e) = F(y)\alpha_S(T_e) + (1 - F(y))\,\alpha_B(T_e), \tag{1}$$

with $F(y) = 2\exp(-y^*)/(1 + \exp(-2y^*)$ and $y^* = (y/\zeta)^2$ (Fig. 2). This is the same function as used in MINIMOS-4 [8] to restrict the surface-roughness mobility to the region near the interface (at $y = 0$).

We have implemented this model for impact ionization in MINIMOS [8] and in MEDICI [9]. The value of the characteristic length ζ has been carefully calibrated from devices of fully scaled NMOS processes with design rules of 0.17, 0.25, 0.35, 0.50 μm (conventional S/D structures) and 0.7 μm (LDD devices). Best fit is obtained for $\zeta = 25$ nm. The measured and simulated I_{sub}– V_g characteristics are shown in Fig. 3 for the deep-submicron generations. Fig. 4 shows the same characteristics for the 0.7-μm generation, where the position of the maximum avalanche rate is at much larger depth than for the deep-submicron generations.

3. Lifetime calculations

The lifetime τ of a MOSFET is usually defined as the time in which the transconductance degrades 10 percent with the gate biased at the maximum substrate current. For these bias conditions, stress experiments show a unique relation between τ and I_{sub}/I_d [1, 2, 3]. Figure 5 depicts τ versus I_{sub}/I_d for MOSFET's with the nominal gate length of different MOS generations. If we use this empirical relation, we can predict the expected lifetime of the transistors. Specifying the minimum lifetime of a MOSFET to be 10 years, the maximum power supply voltage V_{dd} can also be determined. Figure 6 shows the simulated and measured [10] power supply voltage versus the design rule of the MOS generation. For deep-submicron MOS generations, V_{dd} remains constant at 2.5 V [10]. This is caused by the effects of non-local carrier heating. The power supply voltage can remain at fairly high values without affecting the lifetime of the transistor. The agreement between simulation and experiment is excellent.

In conclusion, accurate simulations of the substrate currents over a wide range of MOS generations are only possible with a single model if depth-dependent impact ionization is used together with the energy-balance equation. We have used the same depth dependence as is used for modeling of the surface mobility in MINIMOS-4. Using the simulated drain and substrate currents, the lifetime of MOSFET's can be

predicted from empirical lifetime models. Non local carrier heating is correctly taken into account as is illustrated by the simulation of the constant power supply voltage in the deep sub-micron regime. All the calculations are completely done in post processing after a simple MINIMOS or MEDICI run and consume negligible CPU time.

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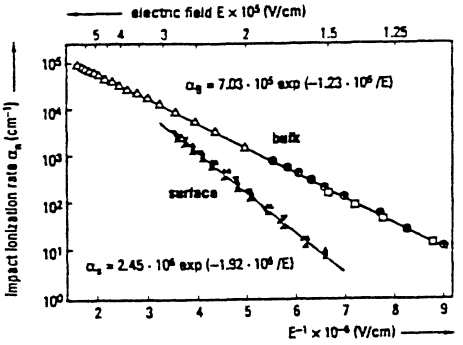

Figure 1: Measured impact ionization rates in the bulk [7] and near the Si-SiO_2 interface [5].

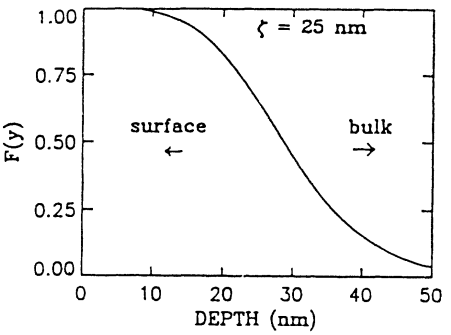

Figure 2: Function used for depth-dependence impact ionization. This function is also used in the MINIMOS-4 mobility model [8].

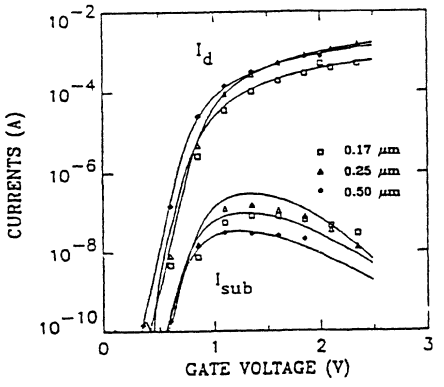

Figure 3: Measured and simulated substrate currents for various MOS generations (design rules 0.17, 0.25 and 0.50 μm). The simulations are done with ζ = 25 nm. For these devices, surface impact-ionization is important.

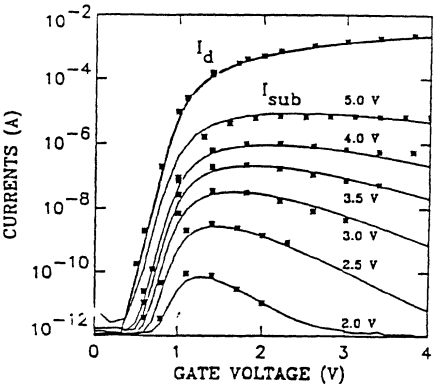

Figure 4: Measured and simulated substrate currents for the 0.70-μm generation (LDD). The simulations are done with ζ = 25 nm. For this MOS generation, bulk impact-ionization is dominating.

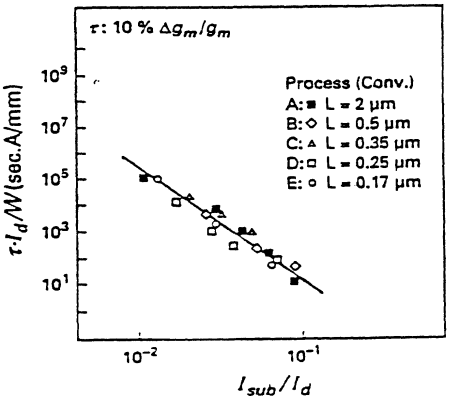

Figure 5: Lifetime plot of τI_d versus $I_{\rm sub}/I_d$ for devices with the minimum gate length of various MOS generations with a conventional S/D. The gate is biased at maximum substrate current. The lifetime criterium is a 10 percent change in the transconductance g_m The data are taken from Ref. [10].

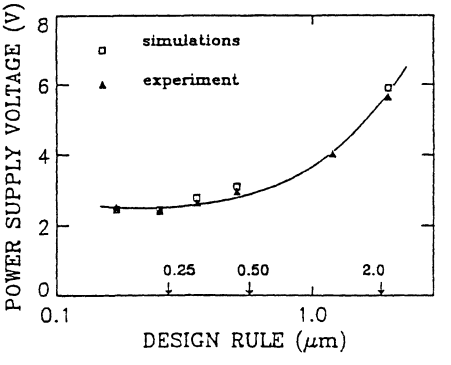

Figure 6: The measured and simulated maximum power supply voltage versus the design rule of the MOS generation. Due to non-local carrier heating V_{dd} remains constant in the deep sub-μm regime. Date are taken from Ref. [10].