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On the Influence of Thermal Diffusion and Heat Flux on Bipolar Device and Circuit Performance

M. Stecher, B. Meinerzhagen, I. Bork, and W. L. Engl

Institut für Theoretische Elektrotechnik, University of Aachen
Kopernikusstraße 16, D-52074 Aachen, GERMANY

Abstract

For device models which consider energy transport the modeling of the flux components due to spatially inhomogeneous carrier temperatures is still a controversial issue. In this paper the influence of these flux components on device and circuit performance is evaluated by the example of a state of the art bipolar technology using mixed level 2D-device/circuit simulation.

1. Introduction

The derivation of hydrodynamic (HD) models from Boltzmann's transport equation (e.g. [1]) depends on a number of approximations (e.g. relaxation time approximation (RTA)) which are of limited validity. Consequently, there is still some controversy concerning the details of the HD models. One of the most controversial issues is the modeling of the flux components driven by the gradients of the carrier temperatures, namely the thermal diffusion (TD) components of the current densities and the heat flux (HF) components (nonconvective parts) of the energy flux densities, respectively. Recently it has been shown that the application of the macroscopic RTA leads to an incorrect modeling of HF and TD under certain conditions [2]. So far the influence of these components on HD device modeling results has been monitored based on unipolar, 1D N^+NN^+ test structures [3],[4], [6].

In this paper, for the first time the influence of TD and HF is discussed based on realistic state of the art bipolar devices and circuits. A related study on the influence of energy transport related effects in general has been published previously [7].

2. The Influence of HF and TD on Device Characteristics

As a test device a realistic, down scaled 2D NPN bipolar transistor structure with a base width of $50nm$ has been selected whose doping profiles (figure 1)) have been optimized to achieve minimal ECL gate delay. All results presented in this paper have been achieved with the simulator GALENE III and the generalized HD model (GHDM) [1]. The GHDM is consistent to an advanced Monte Carlo Model and it has been shown that it reproduces the results of the MC model within short channel MOSFET's very well [5].

For the purpose of this paper the TD and HF components in the GHDM have been modified, so that both components can be independently scaled down using two constant factors f_{td} and f_{hf}, respectively. The modified expressions for the electron current density J and the electron energy flux density S are given below:

$$J = -\frac{q}{m^*}\{\tau_i^* qn\nabla\Psi - \tau_i kT^*\nabla n - f_{td}\,\tau_i n\nabla kT^*\}$$
$$S = -\frac{5}{2q}kT^*\tau_s^*\tau_i^{*-1}\left\{J + f_{hf}\,\frac{q}{m^*}\tau_i n\nabla kT^*\right\}$$

All symbols have their usual meaning as defined in [1]. In order to demonstrate the influence on modeling results caused by either a reduction of TD or HF, three different HD models are compared in this paper: the original GHDM, a modified GHDM with reduced TD ($f_{td} = 0.3$) and a modified GHDM with reduced HF ($f_{hf} = 0.5$). Since it turns out that for all relevant bias conditions holes remain close to thermal equilibrium inside the emitter and base regions, modeling differences for holes are negligible so that in this paper the modeling differences for electrons are predominately demonstrated. The modeling results on the device level are summarized in figures 2-5, respectively. Figure 2 shows the influence on collector current. It can be seen that the early voltage

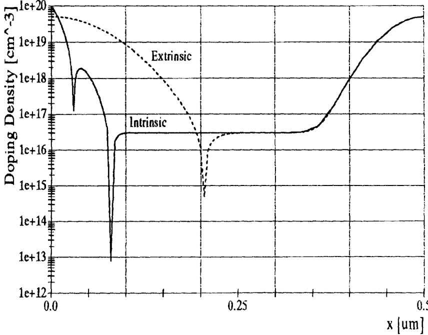

Figure 1: Doping profiles of the bipolar transistor

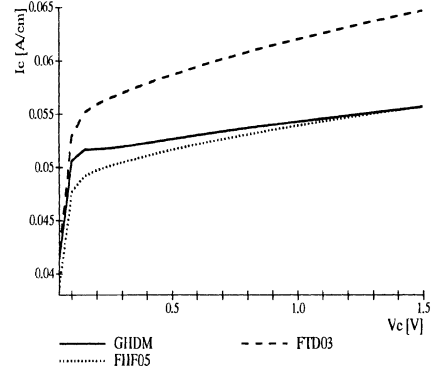

Figure 2: $I_C(V_{CE})$ characteristic for $V_{BE} = 0.8V$

decreases for reduced TD as well as for reduced HF. On the other hand a significant influence on collector current can only be observed by reducing TD. This influence of TD can be understood by analyzing the directions of the two electron diffusion current components within the base region near the emitter. In this region the TD component and the diffusion component driven by the gradient of electron density have opposite directions. Consequently electron injection into the base is increased by a reduced TD component implying a higher collector current. Modeling differences for electron temperature are only minor at least for higher V_{CE} as can be seen in fig. 3. Fig. 4 shows that drift velocity increases at the beginning of the high velocity zone (base collector junction) and decreases at the end of this zone (beginning of the buried layer) when TD is reduced. This is in good agreement with results achieved for N^+NN^+ structures [6]. On the other hand reducing HF has only a minor effect on drift velocity. This is again consistent with [6] because for N^+NN^+ structures reducing HF reduces drift velocity only within the region of the so called "spurious" velocity overshoot peak while only minor drift velocity changes are observed otherwise

and within the bipolar structure of this paper no "spurious" velocity overshoot peak exists. Fig. 5 shows that common base f_t is increased by reducing TD while reducing HF has no influence. The increase of f_t is a direct consequence of the increased current gain for reduced TD.

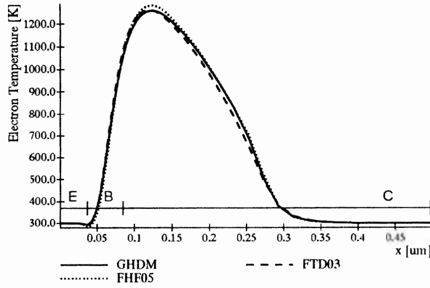

Figure 3: Electron temperature within the intrinsic transistor at $V_{BE} = 0.8V, V_{CE} = 1.4V$

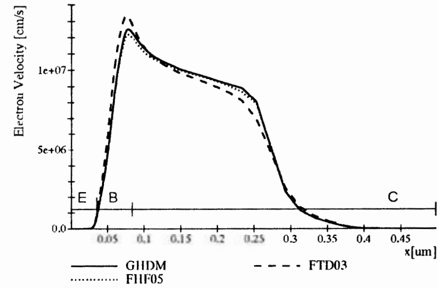

Figure 4: Electron velocity within the intrinsic transistor at $V_{BE} = 0.8V, V_{CE} = 1.4V$

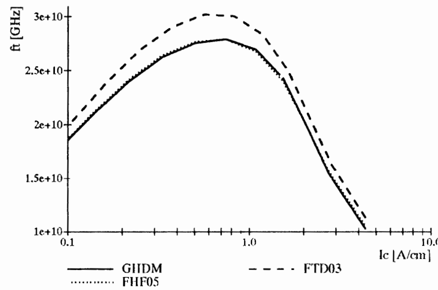

Figure 5: Common base f_T at $V_{CB} = 1V$

3. The Influence of HF and TD on ECL Gate Delay

The consequences of reducing HF and TD for the circuit level are difficult to estimate based on device level results. To overcome this situation the mixed level device/circuit simulation system GALENE III/ CEDUSA has been applied for studying the effects on the circuit level without introducing simplifying assumptions on the device level like in the case of compact models. The ECL inverter circuit analyzed by this simulator system is given in fig. 6. The circuit simulator CEDUSA allows to perform the GALENE III device simulations for the four BJT's within this circuit in parallel, which decreases the required CPU-time drastically [8]. Fig. 7 shows the transient response functions V_{nout} at the inverter output after applying the ramp V_{inp} at the inverter input with the inverter being in steady state before. It can be seen that the differences in the output signals are only minor even in the case of reduced TD.

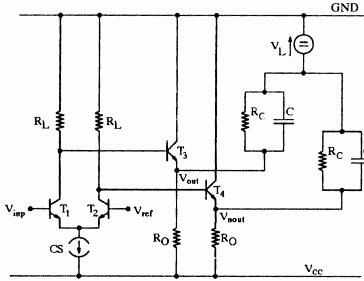

Figure 6: ECL-inverter circuit: $V_{CC} = -3.3V$, $V_{ref} = -1.087V$, $V_L = -1.087V$, $CS = 0.6mA$, $R_L = 0.672K\Omega$, $R_O = 4.036K\Omega$, $R_C = 95.7K\Omega$, $C = 14.2fF$

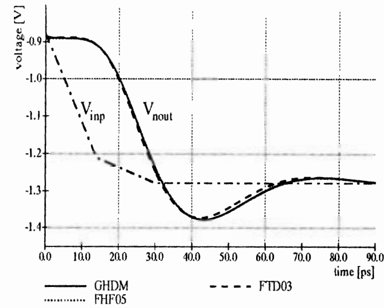

Figure 7: Transient response functions V_{nout} to the applied voltage ramp V_{inp}

4. Conclusion

Though a modified modeling of HF and TD introduces visible modeling differences on the device level, only minor differences can be observed on the circuit level even for devices which are scaled down somewhat beyond state of the art. This implies that presently and in near future an accurate modeling of TD and HF is not necessary for the optimization of ECL circuit performance. However, as soon as further scaling causes the effects already observable on the device level to become significant on the circuit level as well, an accurate modeling of HF and TD is needed.

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