SIMULATION OF SEMICONDUCTOR DEVICES AND PROCESSES Vol. 5
Edited by S. Selberherr, H. Stippel, E. Strasser – September 1993

Electrical Parameter Sensitivity of Deep Submicron and Micron MOSFET Devices with Variation in Processing Conditions

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Abstract

A sensitivity analysis, to examine the influence of processing conditions on device parameters, has been performed and the results are presented here. These results show that effects on micron size devices do not necessarily hold for deep submicron size devices. It is therefore necessary to review to what extent the heuristics which applied for micron size devices are applicable for deep submicron devices.

1. Introduction

Integrated circuit manufacturing is complex because it involves a variety of processing materials and equipment throughout a myriad of processing steps. Each of these steps is a potential source of fluctuations in device characteristics, caused primarily by variations in process conditions, brought about by changes aimed to adjustment, wear, ageing, etc., servicing of equipment, or for example from the purity and concentrations of chemical reactants. Collectively these fluctuations cause variations in the product itself, as for example, fluctuations in the thickness of oxide film grown on the wafer shifting the threshold voltage of any one single transistor. The processing specifications of a wafer are based on parameters developed for a single device. It is therefore important to know to which extent fluctuations of individual process parameters influence the device parameters of the end product. This notion is necessary, not only to decide which processing steps will benefit from tighter control, but also to apply forward correction effectively [1]. While the effects of processing parameters are in the main understood for devices currently produced, little is known about deep submicron devices because little manufacturing experience has yet been accumulated. To gain insight into the effects of process parameters on deep submicron devices a comparative study, between 0.1 μm and 1.0 μm size devices has been carried out. The work is based on simulation using MINIMOS [2]. The structure of the simulation experiment and the results obtained are explained in subsequent sections of this paper.

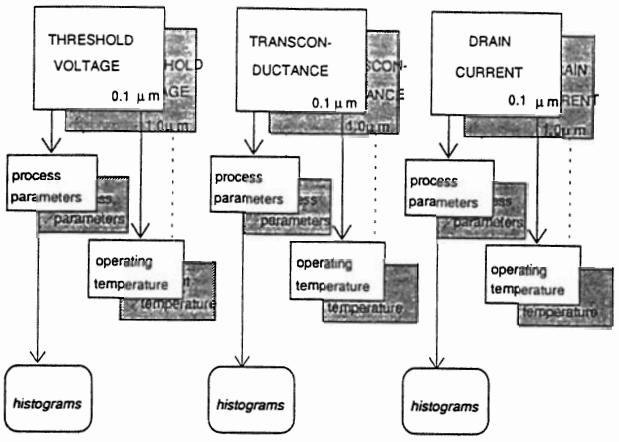

Figure 1: The three main simulation modules of the sensitivity analysis for the considered device parameters, and the operating temperature modules: all simulations were done twice, once for micron (clear front boxes) and once for submicron size devices (shown as shaded background boxes). For each module, comparative histograms were produced with the normalized results

2. Structure of the Simulation Experiment

The function of MOSFET devices is controlled by the joint effects of many parameters and conditions. In our study we have chosen the three main device parameters and operating temperature to be focused on. The device parameters to be simulated were the threshold voltage, the transconductance, and the drain current when the transistor is off. For each of these parameters a simulation module has been implemented to study the variation of any of these device parameter, when the given processing parameter fluctuates in a range typically found in manufacturing. The processing parameters used were gate oxide thickness, gate length, gate oxide charge, bulk doping, and each of the implant parameters for threshold voltage adjustment and source/drain implant: dose, energy, and annealing time and temperature.

The operating temperature is also important to the device because integrated circuits are usually part of other instruments, and thus may have to operate at other temperatures than the optima for which they were. To study this effect another set of simulation modules has been performed.

All the simulations were done twice: for a 0.1 μ deep submicron MOSFETs designed at IBM [3] and for a typical 1.0 μm micron size MOSFET.

Figure 1 summarizes the modular structure of the simulations, showing the submicron device set of simulations modules as clear front boxes, and the micron size device simulation modules as shaded background boxes.

3. Results and Discussion

The purpose of this study is to *compare* the device parameter sensitivity of deep submicron and micron MOSFET devices on processing parameters. In order to establish comparisons a common metric to express processing fluctuations is necessary, thus for each simulation run of a device parameter vs. processing parameter pair the obtained

data were plotted, normalized and fitted. A linear fit was possible in almost all the cases for the plotted data. This is because simulations were done for the relatively small range of fluctuations, typically found in manufacturing, for example $\sigma = 10$ %, that is 20 % or more to either side. The slope of all sets of fitted data was then collected to produce histograms, which make a comparison of the impact of processing parameter fluctuations possible.

Figure 2 shows one such histogram for the threshold voltage. The axis of the histogram measures the sensitivity rate (% vs %) on a processing parameter. Negative sensitivity rates towards the left side, and positive rate towards the right.

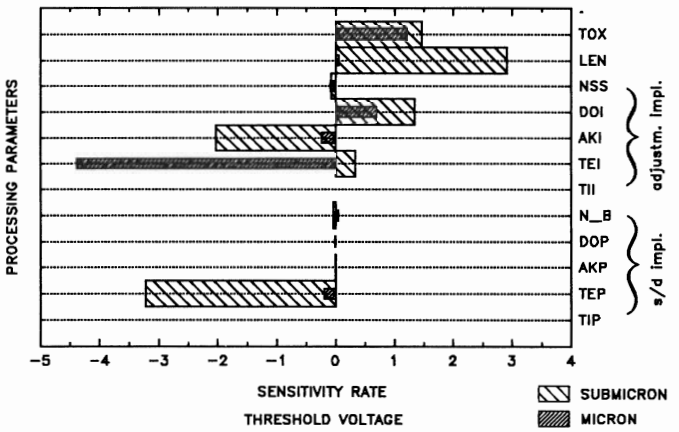

Figure 2: Example of a fluctuation sensitivity histogram

In this study it has been found that a parameter's influencing effect can vary widely: from a strongly influencing parameter in say, micron size devices - to negligible influence in deep submicron devices, or vice versa. For example the implant energy in threshold voltage adjustment is a highly sensitive parameter for the deep sub- micron device, but of little sensitivity for the micron size device. It has also been found that for some processing parameters, a fluctuation - say an increase - can have one effect on a device parameter for one size MOSFETs and the opposite effect for the other size considered. For example a fluctuation of increased oxide thickness causes the off current to increase in the micron size device, it however decreases it in the deep submicron device.

In the case of gate length linear approximation was good for the transconductance, but not for the off current. As can be seen from the figure 3 the threshold voltage and the transconductance sensitivity on the gate length sensitivity is similar for the submicron and micron size device: a 10 % increase in the gate length, as it could happen from slight under etching, causes a decrease in transconductance of approximately 5 % for the deep submicron device, and 7 % decrease for the micron size device.

The off current (drain current, with zero gate voltage) has a completely different sensitivity on the gate length as can be seen from fig 4. For the micron size device it exhibits very little sensitivity to fluctuations (dotted line, left axis scale). For the submicron size device however, it exhibits extremely high sensitivity, but it does not respond linearly (dashed line) to the gate length fluctuation considered. Moreover, we found that this dependence could not be linearized even when the drain current was plotted vs. the reciprocal value of the channel length (1/L). The off current of

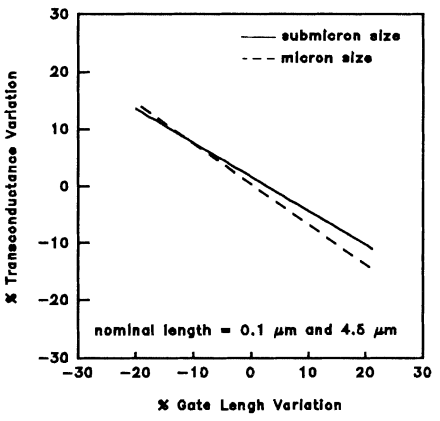

Figure 3: The transconductance sensitivity on gate length fluctuations is similar in submicron as in micron MOSFETs.

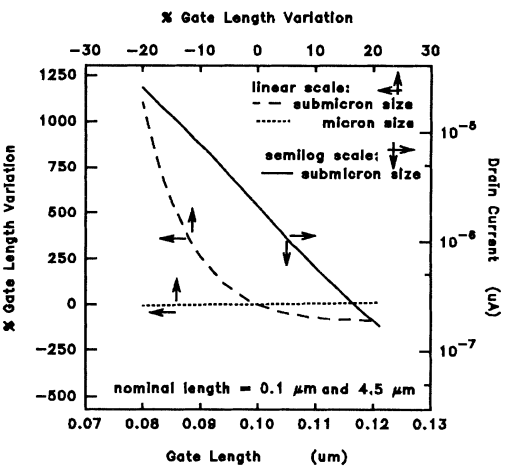

Figure 4: The drain current at $V_g = 0$ is highly sensitive to gate length fluctuation for submicron MOSFETs, but very little to micron size devices.

the submicron device depends exponentially on the channel length (solid line, right axis scale in figure 4) which indicates punch through problems.

4. Conclusion

In this paper a sensitivity study aimed at comparing parameter sensitivity of deep submicron and micron MOSFET devices on processing parameters has been presented. This study shows that parameter sensitivity information is necessary for the advancing submicron technology because the response of device parameters to fluctuations of processing parameters is not necessarily the same as in micron size devices. It is thus important to review to what extent the heuristics which applied for micron size devices, will apply for submicron devices.

References

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