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Efficient and Accurate Simulation of EEPROM Write Time and its Degradation Using MINIMOS

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Abstract

This paper demonstrates an efficient approach to flash-EEPROM write time simulation. MINIMOS is used to simulate the operation of the MOSFET equivalent device consisting of the Si substrate and the EEPROM's floating gate. The effective floating gate voltage is determined analytically using the coupling capacitances and the floating gate charge. With this method write time simulation is performed. Making use of selfconsistent trapping calculation, available in our version of MINIMOS, EEPROM write time degradation due to electron trapping in the gate oxide layer is estimated.

1. Introduction

Stacked double-poly flash EEPROM cells are widely used as devices for nonvolatile memories. Simulation of EEPROM tunneling erase has been performed by replacing the full device structure by a capacitor equivalent circuit [1], [2]. Full transient 2-D device simulation of flash EEPROM write and erase has been reported recently [3], [4]. In the latter case the full device structure is included in the device simulation, making use of charge boundary conditions for the floating gate. As electron injection is assumed to be constant within each time step, small time steps have to be chosen to achieve sufficient accuracy.

In this work we propose a hybrid approach using an equivalent capacitor model and results from the numerical simulation of the MOSFET structure formed by the floating gate and the silicon substrate. We use a modified version of MINIMOS [5] which includes elaborate models for non-local carrier injection and transport in the oxide. In spite of the substantially improved accuracy of gate current calculation, this approach proves to be computationally efficient. Moreover, our models in MINIMOS for oxide carrier trapping and trap generation allow for the selfconsistent calculation of the gate current decrease and the related write time degradation due to trapping of the injected electrons.

2. Models

To model an EEPROM device with MINIMOS (cf. Fig. 1) the equivalent floating gate (FG) voltage V_{FG} has to be determined. We consider the capacitor equivalent

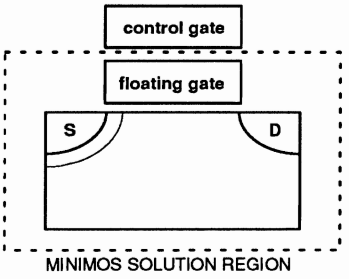

Fig. 1: In the hybrid approach the lower part of the EEPROM device is simulated using the MOSFET simulator MINIMOS.

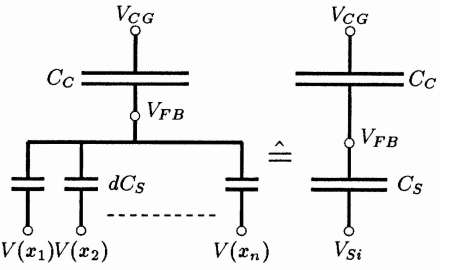

Fig. 2: Capacitor equivalent circuit for EEPROM. C_C is the control gate capacitance, $dC_s = C_{ox}\,W\,dx$ represent the capacitance of an infinitesimal part of the channel.

circuit shown in Fig. 2. It can be shown that an effective voltage V_{Si} can be derived, yielding

$$V_{Si} = \frac{1}{L}\int_0^L \psi_s(x)\,dx + \phi_{ms} \tag{1}$$

representing the average of the surface potential ψ_s along the channel with ϕ_{ms} being the work function of the floating gate material. $V_{Si}(V_{FG})$ (for fixed drain voltage V_D) is extracted from MINIMOS simulations. Fig. 3 shows the result for V_{Si} for a 1 μm device with 10 nm oxide thickness at $V_D = 5$ V. The relation between the FG-charge Q_{FG} and the terminal voltages is found by applying the charge conservation condition. This yields for fixed drain voltage:

$$-Q_{FG} = C_C(V_{CG} - V_{FG}) + C_S(V_{Si}(V_{FG}) - V_{FG}), \tag{2}$$

from which V_{FG} can be determined numerically. C_C is the capacitance between control and floating gate, V_{CG} the control gate (CG) voltage and C_S the capacitance between FG and silicon. During programming of the EEPROM the charge on the floating gate changes due to the gate current I_G:

$$\frac{dQ_{FG}}{dt} = I_G[V_{FG}(Q_{FG})]. \tag{3}$$

The solution of (3), using (2), yields the write time:

$$T_w = -\int_{V_{FG}^{ini}}^{V_{FG}^{end}} \frac{C_C + C_S(1 - \frac{dV_{Si}}{dV_{FG}})}{I_G(V_{FG})}\,dV_{FG}. \tag{4}$$

From this formula it is obvious that for write time calculation it suffices to know the gate current I_G and V_{Si} as a function of V_{FG} (which are taken from MINIMOS calculations). The integral in (4) is evaluated numerically. V_{FG}^{ini} and V_{FG}^{end} are calculated using (2) from $Q_{FG}^{ini} = 0$ and Q_{FG}^{end}, the latter being chosen from the CG threshold voltage target in the programmed state.

The calculation of the gate current I_G is done using a non-local injection formula [5]. The transport of the injected carriers through the gate oxide is described by a

modified drift-diffusion equation. Its solution on the 2-D oxide region provides the current density j_{ox} at every location inside the oxide. Integration of j_{ox} along the gate contact results in I_G. Moreover, j_{ox} can be used together with trap rate equations to model gate oxide degradation due to electron trapping.

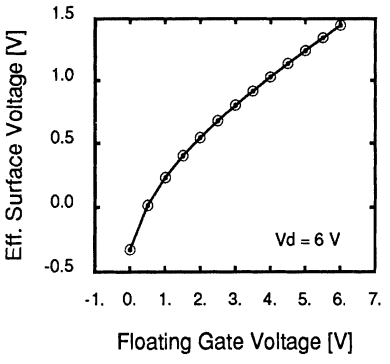

Fig. 3: Effective surface voltage V_{Si} as a function of the floating gate voltage applied in the MINIMOS calculations.

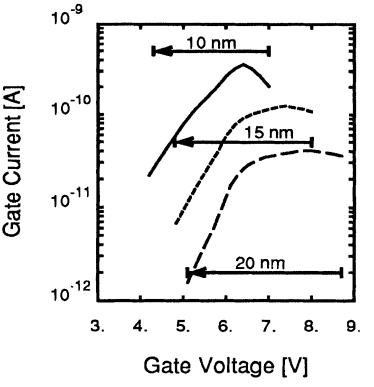

Fig. 4: Gate current as a function of gate voltage for different gate oxide thicknesses at $V_D = 6$ V. The arrows indicate the range V_{FG}^{ini} to V_{FG}^{end} which correspond to $Q_{FG}^{ini} = 0$ and to the charge after EEPROM programming, Q_{FG}^{end}, respectively.

3. Application

In a first application example the model is used to quantify the expected improvement of flash EEPROM programming when the oxide thickness t_{ox} is reduced from 20 nm to 15 nm and to 10 nm. The channel doping was adjusted for each oxide thickness to guarantee the same control gate threshold voltage. The parameters of the injection model were taken from [5]. Fig. 4 shows the simulated gate current and the respective range of I_G-integration. The resulting write times for $V_D = 6$ V and $V_{CG} = 12$ V are 1460, 464, and 160 μs for t_{ox}=20, 15, and 10 nm, respectively.

In a second application the T_w-degradation due to electron trapping in the oxide between the Si-substrate and the floating gate is investigated. Due to electron trapping during the EEPROM write process the electric field in the Si-substrate and thus injection is changed; moreover the local electric field in the oxide layer and thus carrier transport through the oxide is modified. These effects cause a decrease of the EEPROM write current. Our model comprises the following trap mechanisms [6]:

- capture of electrons in bulk traps and oxide field dependent trap to band ionization:

$$\frac{dN^-}{dt} = j_{ox}\sigma \cdot (N_{tot} - N^-) - j_{ox}\beta(E_{ox}) \cdot N^- \tag{5}$$

- oxide field dependent generation of electron traps:

$$\frac{dN_{tot}}{dt} = j_{ox}\gamma(E_{ox}) \tag{6}$$

with N^- being the density of filled traps and N_{tot} the total trap density, σ the capture cross section, β the oxide field dependent trap-to-band ionization efficiency, and γ

the trap generation efficiency. The initial value for N_{tot} is the technology dependent intrinsic trap density. The system of differential equations (5, 6) is solved at every location inside the oxide. The simulation is done selfconsistently, i.e. the change in j_{ox} due to the build-up of oxide charge is taken into account by iterating the calculation of electron injection and electron trapping using appropriate time step control.

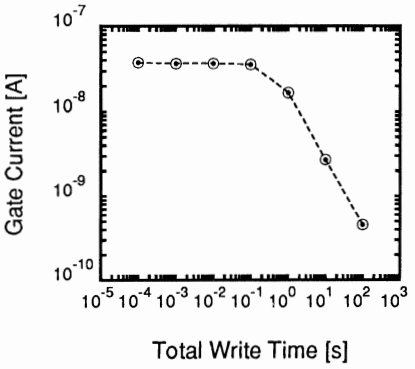

Fig. 5: Degradation of gate current due to electron trapping in the gate oxide as a function of total write time, calculated selfconsistently with MINIMOS.

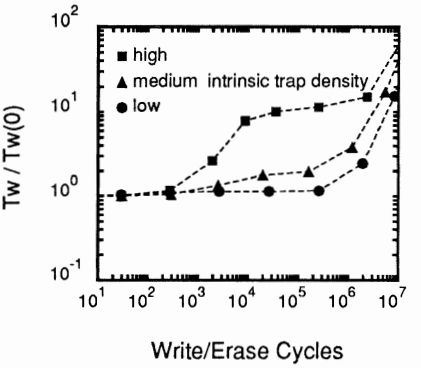

Fig. 6: Relative change of write time T_w as a function of the number of write/erase cycles for different intrinsic trap densities (MINIMOS calculation).

Fig. 5 shows the gate current as a function of accumulated write time. In Fig. 6 the change of EEPROM write time as a function of the number of write/erase cycles is demonstrated for three different values of the intrinsic trap density $N_{tot}(t = 0)$. The increase of T_w after $\approx 10^3$ write/erase cycles is due to electron capture in intrinsic traps, whereas after $\approx 2 \cdot 10^6$ cycles trap generation through hot electron injection becomes important.

4. Conclusion

This work shows that EEPROM write time simulation is efficiently done using a MOSFET simulator and a capacitor equivalent circuit. The gain in computational efficiency can be spent on more sophisticated gate current and carrier trapping models, which allow the investigation of EEPROM write time degradation.

Acknowledgement

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