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Analysis of a CMOS-Compatible Vertical Bipolar Transistor

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Abstract

A vertical npn bipolar transistor (BJT) which can be manufactured in a simple p-well CMOS process without additional process steps is described. The proposed BJT uses a p-well as base and an n^+ S/D doping as emitter. The collector consists of the n^- substrate and does not require an n^+ buried layer or a highly doped substrate. The device is especially suitable for high-voltage applications in electrically hostile environments such as automotive circuits.

1. Introduction

Four different BJT structures (Fig. 1) were designed and analyzed with the two-dimensional device simulator BAMBI 2.1 [1]. Using a high-voltage CMOS process, the S/D junction depth is $1.8\mu m$ and the p-well junction depth is about $6\mu m$, thus, the base thickness is $\approx 4\mu m$ (Fig. 2). The half-cell widths vary from 90μm (structure 1) down to 25μm (structure 4). The characteristics of the optimal structure (no. 4) are: $h_{FE} \approx 160$, $I_{KF} = 0.17$A/cm, $V_{AF} = 170$V, $\tau_F = 0.5$ns. Depending on the application, emitter current densities of more than 1kA/cm^2 can be achieved (limited by the beta roll-off at high collector currents).

2. Collector Resistance

Due to the distributed collector resistance, the BJT exhibits a distinct quasi-saturation behavior which adversely affects the operation at low V_{CE} because of minority injection into the substrate. By optimizing the device, this effect can be kept sufficiently small even without a buried layer. The optimization was performed by reducing both the emitter stripe width and the distance between emitter and collector to a minimum which is determined by high-level injection in the base and the required V_{CEmax} respectively. The vertical doping profile was not changed so that the NMOS and PMOS transistors on the chip are not affected (in particular, the substrate resistivity is confined to 3–5Ωcm). In Fig. 5 and Fig. 7 it can be seen that the structures 3

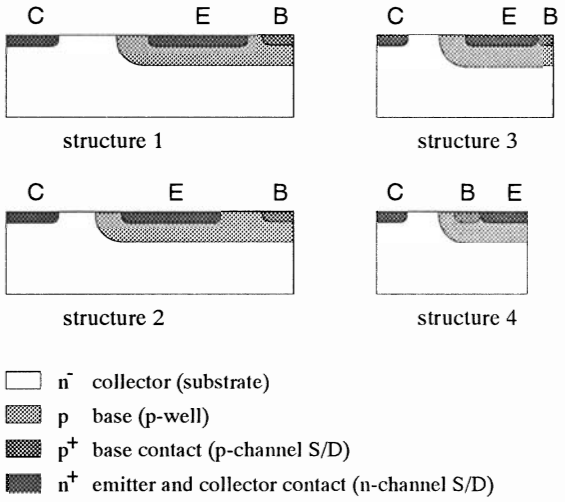

Figure 1: CMOS-compatible BJT structures

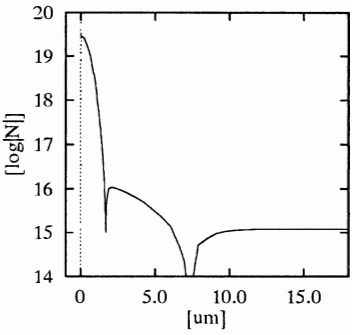

Figure 2: Vertical doping profile [cm^{-3}]

and 4 still exhibit some quasi-saturation which is, however, far smaller than that of the structures 1 and 2. The currents of the smaller structures 3 and 4 were scaled so that the comparison refers to the same total device area.

3. High-Voltage Capability

The placement of the base contact has an essential impact on the dynamic and high-voltage behavior: The lateral part of the transistor limits its overall high-voltage performance due to the higher electric field at the surface, which is responsible for punch-through, especially, when steep pulses are applied to the collector (structures 1–3). However, if the base contact is placed between collector and emitter (structure 4) the p^+ doping at the base contact virtually eliminates the lateral BJT, which allows for higher V_{CE} and reduces the avalanche multiplication current at the surface. Additionally, the effective base resistance is reduced which also enhances the dynamic and high-voltage behavior. Fig. 6 shows the output-characteristics of the four structures for high V_{CE}. The structures 1 and 2 suffer mainly from their high effective base resistance. The maximum V_{CE} of structure 3 is limited by the avalanche generation in the base-collector junction at the surface.

4. Applications

The BJT is used in a supply protection circuit for static and dynamic overvoltage protection. The circuit must handle a permanent overvoltage of 24V d.c. and pulses of up to 80V at $t_r = 1\mu s$ at a nominal load current of 300mA/cm. It consists essentially of a series regulator which limits the internal supply to $\approx$16V (Figs. 3, 4). The BJT must not saturate at all, otherwise it would be a bypass for steep overvoltage pulses. As the collector is contacted to the substrate, the circuit needs Zener diodes on its output too.

Fig. 8 shows the behavior of the four structures in the case of a steep V_{CE} pulse at the nominal load current ($R_B = 0$). The structures 3 and 4 can easily handle the pulse whereas the two wider structures 1 and 2 are overloaded due to saturation. A finite resistance R_B in the base branch has no detrimental effect because the additional voltage drop across R_B reduces the minority injection into the substrate so that the voltage overshoot is virtually not increased by the base resistor.

Further possible applications of the BJT which can also be merged with PMOS transistors include amplifiers, shunt regulators, buffers, solenoid drivers, and stepper motor drivers.

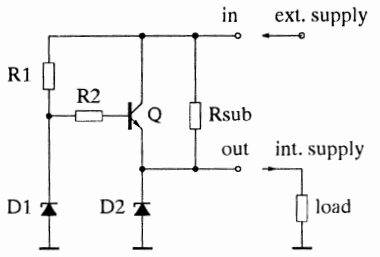

Figure 3: Series regulator as overvoltage protection circuit

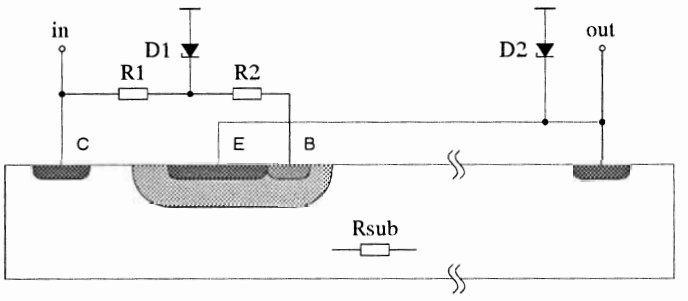

Figure 4: Integration of the protection circuit with structure 3

References

[1] W. Kausel, G. Nanz, S. Selberherr, H. Pötzl, *BAMBI - A transient two-dimensional device simulator using implicit backward Euler's method and a totally self-adaptive grid*, NUPAD II Workshop, May 9–10, 1988, San Diego, Ca., Digest No. 105/106.

[2] F. Berta, J. Fernandez *et al.*, *A Simplified Low-Voltage Smart Power Technology*, IEEE Electron Device Lett., pp. 465-467, 1991.

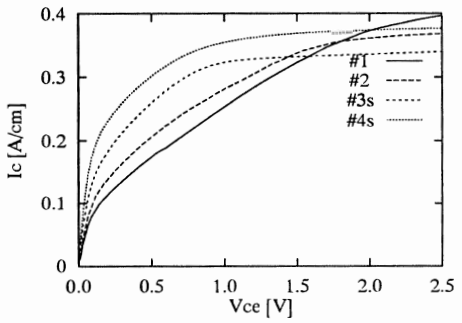

Fig. 5: Output-characteristics for different structures

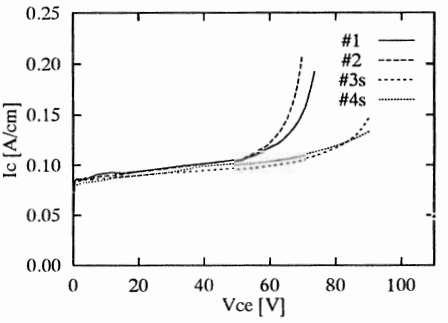

Fig. 6: Output-characteristics for different structures

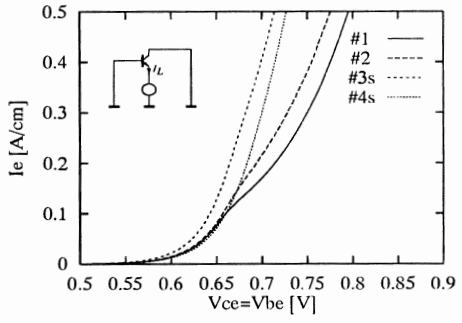

Fig. 7: Voltage drop vs. load current for different structures

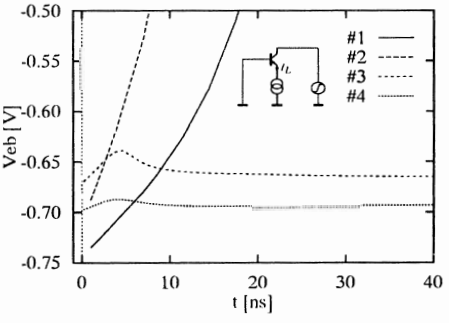

Fig. 8: Voltage overshoot at 80V/us, I=300mA/cm for different structures

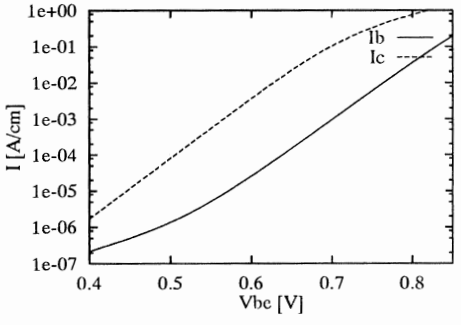

Fig. 9: Input-characteristics of structure 4

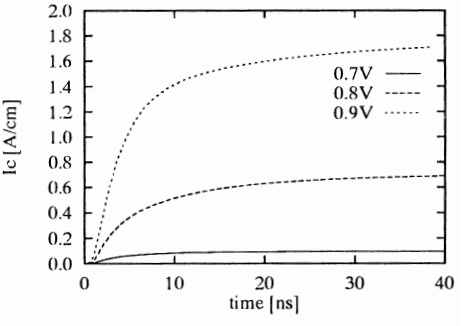

Fig. 10: Turn-on characteristics of structure 4 for different Vbe pulses (tr=1ns), Vce=10