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Simulation of a Novel Scheme for 700-1000 V Wiring Applications

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Abstract

This paper investigates an isolation and wiring scheme for a typical 700–1000-V, junction isolated (JI), high voltage integrated circuit (HVIC), process. The 2-D device simulator S-PISCES2B [1] is used to simulate the behaviour of the isolation, and that of a novel wiring technique used to run high voltage wires over the isolation.

1. Introduction

A common problem in today's high voltage integrated circuit (HVIC) technology is the ability to route metal wires around the chip. A 200-V wiring scheme has already been investigated by the authors [2]. Studies have also been carried out by other authors in the 400-V range [3]. However, I.C.'s in the 700–1000-V range are now been fabricated using junction isolation [4], and these are particularly vulnerable to parasitics induced by high voltage interconnect on chip. If figure 1 is examined, ignoring the field plates and p- extension, a general wiring problem is illustrated. The n+ drain of a high voltage device (e.g. an LDMOS), must be connected to other circuit elements, requiring a high voltage wire to run across the isolation. This paper uses the 2-D device simulator S-PISCES2B [1] to investigate isolation and a novel wiring scheme for a typical 700–1000-V HVIC that might be used in a.c. off-line applications.

2. Simulation structure

The general simulation structure is shown in figure 1. The epi layer is represented by uniform doping and the profiles by 1-D gaussians rotated by a lateral ratio of 0.7. The wire was simulated by placing an aluminium contact on top of a $3\mu m$ oxide. Field plates fp1–fp3 represent biased polysilicon field plates connected by biasing resistors. For simulation purposes, the resistors were ignored, fp1–fp3 were defined as n-type poly contacts and the required potential was placed directly on the field plate. The structure in layout is shown in figure 2, without the field plates. Simulation has been carried out using the 2-D device simulator S-PISCES2B [1]. Wiring has been investigated for the case of a $20\mu m$, $8 \times 10^{14} cm^{-3}$ n-type epi layer on a $1 \times 10^{14} cm^{-3}$ p-type substrate. Breakdown of the p+ isolation/n-epi diode was modelled using the full

two carrier impact ionisation model with ionisation coefficients of Van Overstraeten and De Man [5]. A rectangular mesh was used to eliminate the generation of obtuse triangles by the regrid statement, and to keep the number of nodes at a minimum. The total number of nodes used was 1476, with a spacing ratio of $0.667 < x < 1.5$.

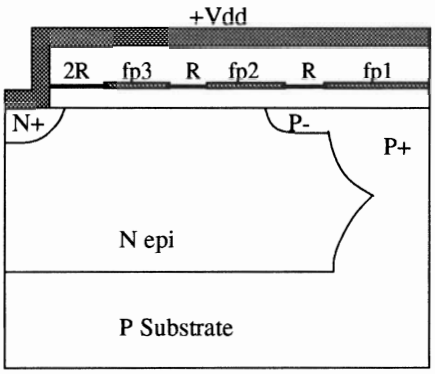

Figure 1: Field plate scheme.

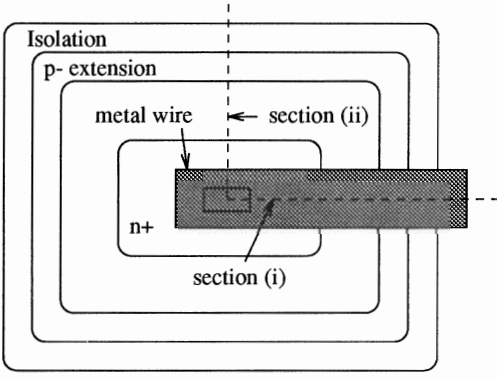

Figure 2: Layout of wiring structure.

3. Simple isolation structure

The breakdown of the p+ isolation/n-epi junction was simulated as 681-V without the wire. When the n+ contact was extended to run over the isolation, it was found that field crowding at the surface near the p+ edge caused the breakdown to drop to 229-V. This compares well with a previously published value of 180-V [6]. A p- extension can be used to reduce the field crowding at the p+ isolation edge [6]. This is shown clearly in figure 3, where we can see the potential contours moved from the p+ edge and distributed evenly across the p- extension.

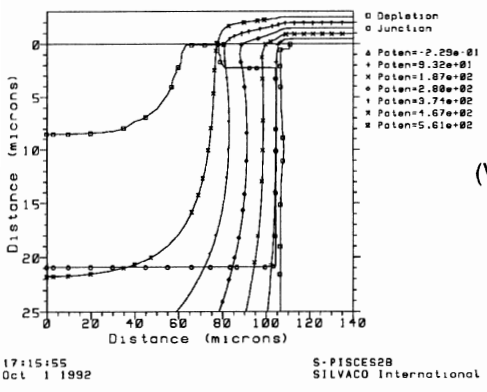

Figure 3: P- extension effectively prevents potential crowding at p+ edge. Wire is at 560-V.

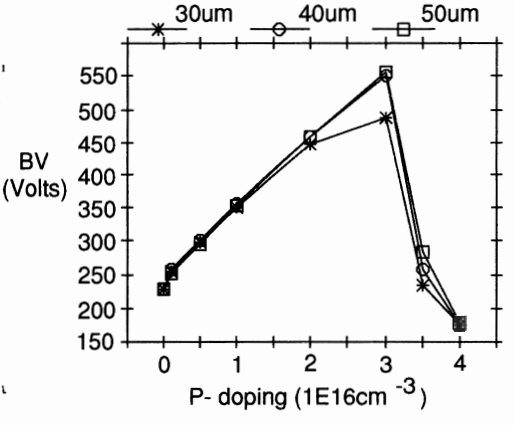

Figure 4: Breakdown vs p- doping for three different extensions. Extension is the drawn distance between the p-/p+ edges.

Breakdown versus p- doping for three different extensions is shown in figure 4, the optimum being a drawn extension of $40\mu m$ at a peak doping of $3 \times 10^{16} cm^{-3}$. At low dopings, the extension depletes too quickly, and the breakdown approaches that of the p+ value. At high dopings, the extension depletes slowly, and breakdown moves from the p+ region to the edge of the p-. The optimum extension gives a breakdown of 550-V with the wire.

4. Wiring structure

In order to obtain 1000-V wiring, biased polysilicon field plates are used to redistribute the electric field along the surface. In a real structure, the field plates would be inserted as rings between the p- extension and the n+, and be biased as a function of V_{DD} using a voltage division scheme. The structure is shown in figure 1. For simulation purposes, the resistors are ignored and the required potential is placed directly on the field plates. The voltage on the electrodes is stepped until the required potential for each one is reached. Stepping each electrode as a multiple of V_{DD} would have been more realistic, however this was too cpu intensive, as the algorithm would only allow estimates from one previous solution.

Since the field plate over the isolation (fp1) is grounded, the inter-layer dielectric needs to sustain the full drain voltage. Here the simulation just monitors the oxide field. The field plate fp3 is biased at approximately $V_{DD}/2$ and fp2 at approximately $V_{DD}/4$. The distribution of the potential contours is shown in figure 5, with the wire V_{DD} at 880-V, fp3 at 480-V, fp2 at 240-V and fp1 at 0-V. Also shown in figure 5 are impact ionisation contours, illustrating areas of maximum field crowding, and total current vectors, showing the flow of carriers generated due to impact ionisation. We can see that breakdown occurs at the surface. A p- extension of $5 \times 10^{15} cm^{-3}$ was used. The breakdown voltage of the non-wire part of the structure, (illustrated by section (ii) of figure 2), was also simulated. Using the same p- extension of $5 \times 10^{15} cm^{-3}$, the breakdown voltage was increased from 681-V to 1340-V. Potential contours for this structure are shown in figure 6.

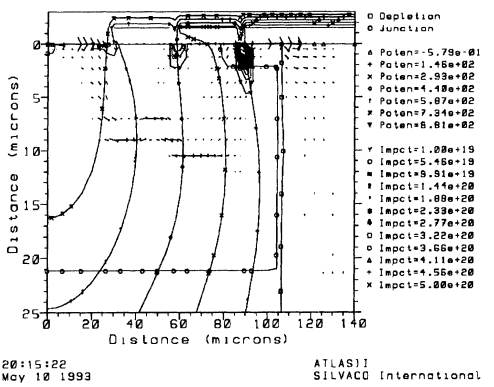

Figure 5: Potential and impact ionisation contours in field plate structure at 880-V. Also shown are total current vectors. Corresponds to section (i) of figure 2.

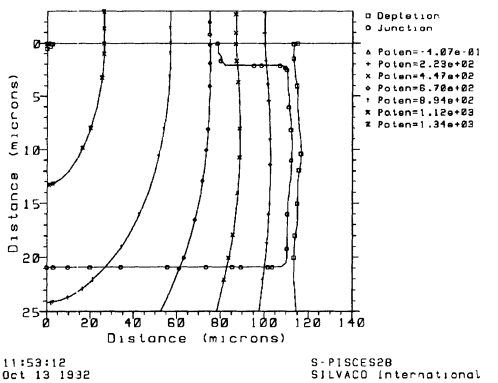

Figure 6: Potential contours of structure without wire and with a p- extension of $5 \times 10^{15} cm^{-3}$ at 1340-V. Corresponds to section (ii) of figure 2.

5. Limitations of simulation

As the field plate voltages were not stepped as multiples of V_{DD}, the potential distributions in going from 0-V to breakdown would be different in a real device.

The simulation only monitored the oxide field, and did not account for failure mechanisms that may occur in a real oxide.

Also, the simulation only modelled a 1-D field plate, as shown by section (i) of figure 2. The wire was assumed to have infinite lateral geometry whereas a real wire would have a finite dimension. 2-D edge effects were therefore ignored. However, since the width of the wire in a real structure is small in comparison to the overall size of the device, it may be the case that the electric fields under a real wire may not be as dominant as those simulated here.

6. Conclusions

A simple optimised p- extension can increase the breakdown of an isolation structure with a wire running over it from 229-V to 550-V. To obtain isolation greater than 800-V, biased polysilicon field plates can be used to redistribute the critical electric fields. The p- extension used here can increase the breakdown of the non-wired part of the structure from 681-V to 1340-V.

References

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