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Charge Distribution and Capacitance of Double Barrier Resonant Tunneling Diodes

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Abstract

Charge and potential profiles are self-consistently calculated in double-barrier heterostructures to derive the capacitance of resonant tunnelling devices. We show that the dipole charge integrated over the accumulation or the depletion side of the device is the result of a complex arrangement of the mobile charge dragged and drifted when a bias is applied. Excellent agreement is found with capacitance measurements carried out on high performance resonant tunnelling diodes up to 40 GHz .

1. Introduction

The resonant tunnelling effect through double barrier heterostructure is an intrinsically fast process which is currently used in the proposal of new high speed devices. For this application view point, it is essential to predict how the charges are distributed within the heterostructure, notably to derive the tunnelling conductance and the intrinsic capacitance of the device and hence its frequency capabilities. Basically, several interdependent processes are involved in the arrangement of the mobile charge. This includes diffusion phenomena from the highly doped contact regions and the accumulation effects of carriers in the emitter and in the well regions respectively. In addition, the situation is complicated by the fact that the structure consists of quantum zones with a two-dimensional density of states D(E) and of semi-classical regions acting as reservoirs of electrons with monotonous variations of D(E).

In this paper, the problem of the charge distribution in resonant double barrier heterostructure is more especially addressed. After discussing the various effects involved in a generic sample, we report the conduction band and the internal electric field profiles we calculated in the Thomas-Fermi approximation, i.e. carriers concentrations determinated assuming Fermi-Dirac statistics and constant Fermi levels within each contacts. Theses results were validated by comparison with more sophisticated formalisms. Lastly, to test the model, we designed and fabricated Double Barrier Heterostructures (D.B.H.) with very thin barriers. Their capacitance variations measured up to 40 GHz are in very good agreement with those predicted by simulations .

2. Charge arrangement

In figure 1, we reported the typical band bending we got for a resonant tunnelling diode which consists of AlAs/$In_{0.53}Ga_{0.47}As$/AlAs D.B.H. (structure A). Moreover , this tunnelling structure is cladded between two spacer layers with a stepped doping profile to provide electron reservoirs and to make possible the formation of low resistance contacts. Except for the diffusion potential due to the gradient of doping, one can note

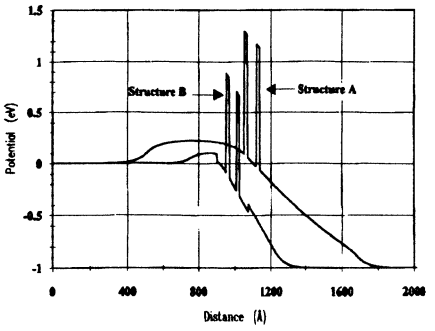

Figure 1 : Conduction Band Edges at 1 V for structure A and B

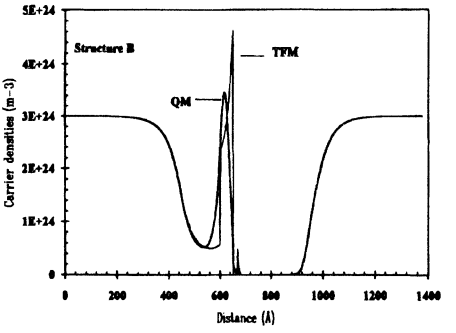

Figure 2 : Carriers densities under bias with 2 models : TFM and QM

that an accumulation zone forms in the front of the D.B.H . In contrast , at the right hand side, the spacer layer is partly depleted . In practice, the calculation of such a profile raises a number of fundamental issues i.e. how the charge is shared between the different regions.

First of all, we have to stress that the amount of charge trapped in the well is small because we used symmetric ultra-thin barriers for increasing the current density , a welcome feature for high speed applications. It results from this that the carrier lifetime on the ground state is very short and hence the sheet carrier density n_S trapped in the well. Confidence in such an assertion can be found through Wigner distribution function simulation which gives a direct evaluation of n_S [1]. A maximum value of 5 10^{10} cm^{-2} was thus found at the peak voltage for a peak current density of 60 kA/cm^2 in agreement with aforementioned arguments [2]. Concerning the emitter-accumulation layer , the situation is not so straightforward. In fact, the problem that faces us is that the net charge is the superposition of a 3D contribution due to the extended states and a 2D component due to the electrons in the triangular-shaped potential. This 2D injection is exemplified in figure 1 which also gives the band bending for a strained InGaAs/GaAs/AlAs heterostructure (structure B). Such a pseudomorphic structure enforces the two-dimensional (2D) character of the carrier injection due to the presence of a pre-well prior to the first barrier [3], whereas, the undoped prewell controls the escape process and the postwell is grown to preserve symmetry .

At this stage, it is interesting to compare the carrier distribution obtained by a self-consistent calculation between the Poisson equation and the carrier concentration n(z) calculated classically (Thomas-Fermi Model) and by the Schrödinger equation for the two dimensional states (Quantum Model) . Such a comparison is made in figure 2 . Despite the fact that a Thomas-Fermi model gives rise to unphysical jumps in the carrier distribution , it was found that the variation against voltage of the integrated charge over distance is conserved and hence the capacitance of the device. From the conduction

profile given above , we can also derive the internal electric field F and determine the peak values of F and the screening length. The results we obtained for structure A at various bias voltage are reported in figure 3. At the interface between the $4 10^{18}$ cm^{-3}

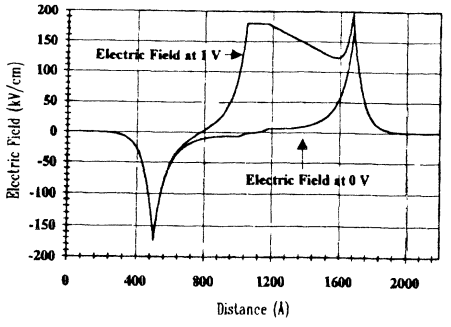

Figure 3 : Electric Field Profiles at 0 and 1 V for structure A

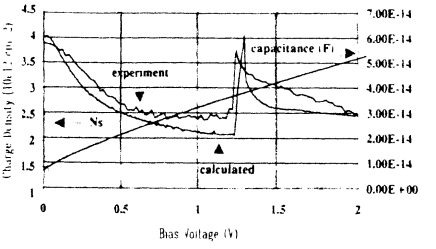

Figure 4 : Charge density and calculated capacitance versus bias voltage

doped layer and the spacer layer with a doping concentration of 10^{17} cm^{-3} , the electrical field reaches values as high as 170 kV/cm. As a general rule, this field is screened over relatively long distance comparable to the thickness of spacer layers. Under bias , the situation appears more complex with a close interdependence of the diffusion field and of the internal field in the quantum zone. This lack of separation between the different physical processes complicates notably the numerical procedure. Here , the simulation code we used is a double sweep routine (Choleski code) which reveals very efficient for realistic potential profile .

3. Capacitance

From the conduction band profile, the electrical properties (tunnelling conductance and capacitance) can be directly evaluated by solving the Shrödinger equation throughout the structure and thus get the tunnelling transmission probabilities [4] and by summing the charge either in the emitter or the collector side [5]. Here, we focus our attention on the second issue. Figure 4 gives the variation of the integrated charge up to the first hetero-interface leading to the potential profile given in figure 1 The calculated capacitance values, $C = A\partial Q / \partial V$, with A the diode area , is also given For A = $20\mu m^2$, corresponding to the samples we fabricated, the capacitance values Cmax is 60 fF. For comparison, a simple parallel plate capacitor with a dielectric thickness limited to the double barrier will lead to a value exceeding Cmax by a ratio of 4. At increasing bias, the sheet density monotonously increased with a quasi-linear variation above 0.5 Volt. The value Cmax/Cmin obtained in that case is of about 2. The calculations reported before were made assuming that no current will flows through the device. One can expect that the introduction of the mobile charge forming the current will drastically affect the capacitance, when the diode is-in or out-of resonance. Such an effect can be simply introduce using the conductance of the diode and a mean velocity [6]. The results obtained in that case are shown in figure 4 .

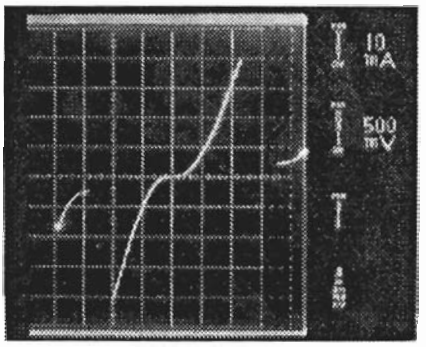

Figure 5 : Typical I(V) curve at 300K (A=100μm2) for structure A

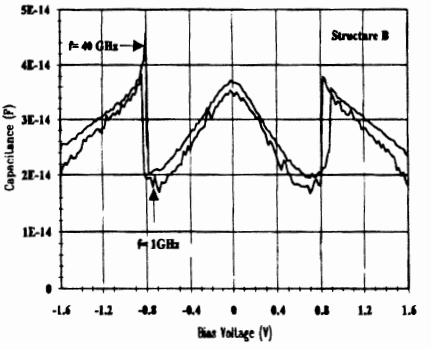

Figure 6 : Capacitance values of Structure B (A=20μm2) at 1 and 40 GHz

4. Comparison with experiment

Structures A (AlAs/GaInAs) and B (GaInAs/AlAs/GaAs) were grown by molecular beam epitaxy . In order to have a direct evidence of the intrinsic capacitance effect, the device were fabricated in a low parasitic technology we developed previously. Details of fabrication procedure can be found elsewhere [7]. The devices exhibit excellent D-C performances with a nominal peak to valley ratio Jp/Jv of 9:1 and a peak current Jp of 30kA/cm^2 for structure A whereas Jp/Jv and Jp were typically 7 and 50 kA/cm^2 for structure B. For example , figure 5 gives a typical I-V curve measured at room temperature from which the tunnelling conductance can be deduced. We reported in figure 6 the variations of the capacitance measured at 1 and 40 GHz respectively for structure B. Similar C(V) variations are obtained proving the inherent fast response of the structure. Besides , by comparing the numerical and experimental data of figure 4, a good agreement is now obtained over the voltage range investigated.

5. Conclusion

In summary, the capacitance-voltage relationship of resonant tunnelling diode was successfully obtained by performing calculations based on the self consistent approach of the charge and potential distribution. The Cmax and Cmax/Cmin values are due to the variation of the charge density and the sudden increase near peak voltage is attributed to the tunnelling current flow.

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