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Mechanical Stress Simulation During Gate Formation of MOS Devices Considering Crystallization-Induced Stress of p-Doped Silicon Thin Films

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Abstract

Mechanical stress in silicon substrates caused by thin-film deposition of gate material of MOS transistors is analyzed by the finite element method. The results reveal that to predict precise stress distribution, it is very important to take into account the intrinsic stress of the thin films used as gate material as well as thermal stress .

1. Introduction

With the trend towards high integration of LSIs, it has become increasingly important to minimize or control the mechanical stresses that occur in LSI device structures during manufacturing processes [1]. This is because the device structure has become very complicated, with a lot of sharp corners, where mechanical stress easily concentrates. In addition, newly employed gate materials of MOS transistors, such as P-doped poly-Si films and WSix films, are found to hold very high intrinsic stress of about 1000 MPa [2]. Thus, the internal stress of the new device has been increasing drastically, causing not a few mechanical failures such as film cracking, delamination, and dislocation generation in silicon substrates. Since these failures deteriorate device characteristics, they have to be eliminated during manufacturing. These mechanical failures have been eliminated by many trial and error efforts, but it usually takes more than several months to find an appropriate countermeasure. To minimize device development cost and time, a mechanical stress design system has been developed by applying finite element analysis and stress measurement [3]. The system consists of three subsystems: an experimental database construction system, a stress simulation system and a stress evaluation system. This system is effective for optimizing both device structure and manufacturing process without mechanical failures. In this paper, stress optimization of MOS (metal oxide semiconductor) structures using P-doped Si thin films as gate material by applying this system is discussed .

2. Stress measurement of gate materials

The internal stress of thin films used as gate material was measured by detecting changes in substrate curvature after film deposition. A scanning laser microscope was used for the curvature measurements. P-doped silicon thin films and WSix ($2.4<x<2.7$) thin films were deposited on 10-nm thermally oxidized silicon wafers by chemical vapor deposition

Specimens were cut from the wafers as strips, 30-mm long, 3-mm wide and 0.55-mm thick. The resolution of the stress measurement was about 15 MPa.

An example of data obtained from the phosphorous of 4E20/cm^3-doped silicon thin film 150 nm thick is shown in Fig. 1. The abscissa is temperature and the ordinate is the internal stress of the film. In this case, the film was deposited in an amorphous phase and held compressive stress of about 200 MPa. During crystallization of the film, the internal stress changed drastically to tensile stress of about 600 MPa at about 600 °C. This stress change is due to volume shrinkage of the film. The developed stress decreased with annealing at temperatures above 700°C because of the viscoelastisity of the film. On the other hand, the internal stress of the conventional $POCl_3$ treated polysilicon thin films did not change from the initial tensile stress of about 300 MPa during annealing. Therefore, it is important to choose the annealing temperature so as to control the internal stress of the P-doped silicon thin films.

Figure 2 shows example internal stress changes of 150-nm thick WSix thin films. Though the initial stress depends on the film deposition temperature, the final stress after 900 °C annealing reached the almost constant value of 1500 MPa. The stress change of the film deposited at 400°C occurred during silicidation due to volume shrinkage of the film.

3. Stress simulation

Mechanical stress was simulatedusing the finite element method [4]. To take into account the internal stress of thin films, Maxwell's viscoelastic model was modified as shown in Fig. 3. In this model, the stress-strain relationship can be expressed as

$$\Delta\sigma = (D + \Delta D)(\Delta\varepsilon - \Delta\varepsilon_\theta - \beta\Delta\varepsilon_v) + \Delta D \cdot D^{-1}(\sigma - \sigma_i),$$

where, σ is stress, σ_i is internal stress of the film, ε is the total strain, ε_θ is thermal strain and ε_v is viscous strain. D is the material moduli matrix and D^{-1} is its inverse matrix. β is the elastic ratio of Young's moduli, E_1 and E_2. The internal stress is treated as initial strain, which is assumed to be a parallel term of the model (Fig. 3). In this model, the internal stress is a function of temperature to take into account the internal stress change of thin films.

The model MOS structure is shown in Fig. 4. In this model, P-doped silicon and WSix films are integrated as the gate material. The space between two gates is fixed at 0.7 μm. The gate width effect on the substrate stress is analyzed. An example of the predicted stress is shown in Fig. 5. The abscissa is the gate width and the ordinate is the averaged normal stress along the gate width direction. The predicted stress is averaged in the area of the gate space region, 0.7 μm in width and 0.5 μm in depth, because of the spatial resolution of stress measurement using microscopic Raman spectroscopy [5]. The predicted stress without considering the internal stress of films, i.e., considering only thermal stress, differs completely from the measured result. The predicted thermal stress shows little gate width dependency on the substrate stress, but the predicted result considering both thermal stress and the internal stress of both films agrees very well with the measured result. This example clearly indicates that the residual stress in the substrate after gate formation using P-doped silicon and WSix films is mainly determined by the internal stress of the films. It is important, therefore, to take into account the internal stress of thin films in order to obtain precise simulation results.

4. Optimization of gate formation process

The leakage current level of a MOS structure between N^+ drain and p-type substrate using the P-doped silicon film as gate material was evaluated (Fig. 6). When the annealing temperature after the deposition of the gate was lower than 800°C, abnormal leakage current was measured, whereas the leakage current level of the MOS structure using the conventional $POCl_3$ treated polysilicon film was low and stable. The abnormal leakage current was caused because the dislocations that were generated and grew at the gate edge after the annealing.

To discuss the dislocation generation mechanism, stress simulation of the MOS structure was performed by considering the internal stress change of the P-doped silicon films as shown in Fig. 1. The predicted substrate stress at the gate edge is summarized in Fig. 7, where the abscissa is the annealing temperature and the ordinate is the normalized resolved shear stress along [111] slip plane. In this case, the stress level predicted from the conventional $POCl_3$ treated polysilicon gate is used for the normalization. As shown in this figure, the substrate stress level at the gate edge increases with lowering annealing temperature. Dislocations were observed when the stress level exceeded 2.0, i.e., the annealing temperature was lower than 800°C. To eliminate dislocations, the annealing temperature was set at 950°C. Applying the revised process, the leakage current level became low enough to assure device reliability, as shown in Fig. 8. No dislocations were observed at the gate edge after 950°C annealing. It is concluded that the mechanical stress design is very important in improving both the device and the process reliability.

5. Summary

Mechanical stress simulation was performed with the aim of eliminating dislocations at the gate edge of MOS structures using P-doped Si and WSix thin films. It is very important to take into account the internal stress of the films so as to obtain precise simulation results.

Acknowledgements

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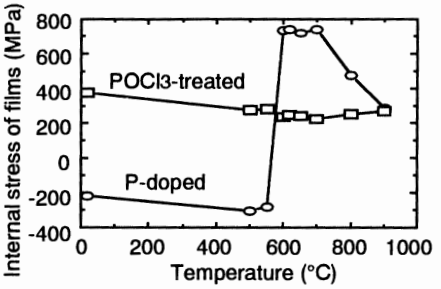

Fig. 1 Internal stress change of Silicon thin films

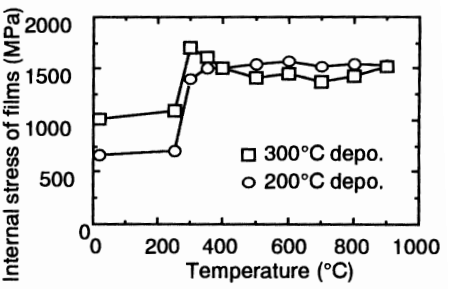

Fig. 2. Internal stress change of WSix thin films (2.4<x<2.7)

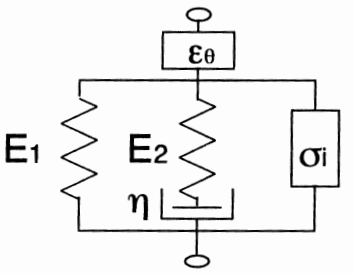

Fig. 3. Maxwell's viscoelastic model

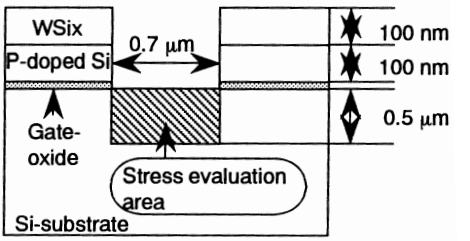

Fig. 4 Model MOS structure

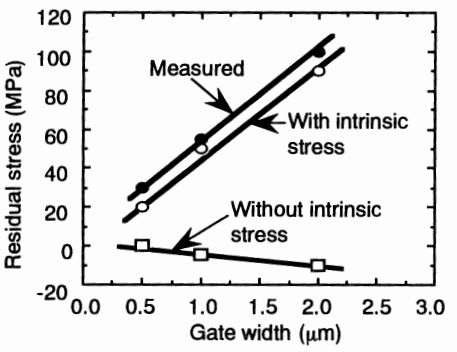

Fig. 5 Preicted gate width effect on substrate stress

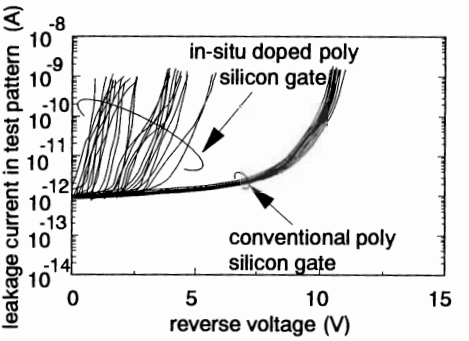

Fig. 6. Junction leakage current between N+ drain and P-type substrate of MOS structure after 800°C annealing

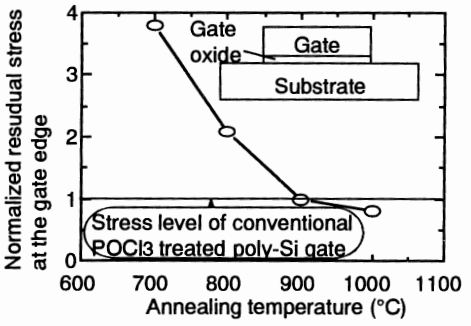

Fig. 7 Predicted annealing temperature dependence of the substrate stress at the gate edge.

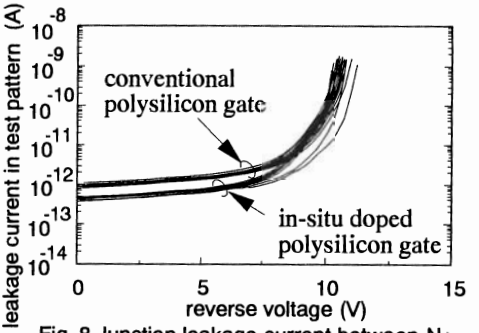

Fig. 8 Junction leakage current between N+ drain and P-type substrate of MOS structure after 950°C annealing