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Process Optimization in a Production Environment Using Simulation and Taguchi Methods

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Abstract

This paper discusses the use of Taguchi Method in conjunction with process simulation for optimising IC processes in a high volume production environment. The use of orthogonal arrays is presented and two applications detailed.

1. Introduction

In the past, process and device simulation has been routinely used in R&D laboratories, but this has not been the case in the production environment. However, structured experimentation is widely used in manufacturing plants with Taguchi methods being very popular. This paper describes the application of simulation in conjunction with Taguchi methods to two problems experienced in a high volume production facility. While both of the examples are relatively simple they do demonstrate that simulation, when used with Taguchi methods, has the potential to save a significant amount of money as well as speed up the time taken to identify the causes of problems.

2. The Taguchi Method

The Taguchi method has been the subject of much interest over recent years [1]. While statisticians have argued about its merits there is a plethora of papers that report successful applications [2, 3]. The method uses orthogonal arrays [4] to reduce the number of experimental runs required to characterise a process. These arrays have special properties that allow the effect of control factor upon responses to be calculated. An example of an orthogonal array which can be used to examine the effect of control factors A to G is given in table 1.

Each of the control factors has two level settings and the effect these have upon the output responses is easily determined because the orthogonal array has been designed to effectively balance out the influence of all the other factor settings. For example the effect of level setting 1 of control factor A is simply obtained by calculating the average of experiments 1, 2, 3 and 4. Similarly, the effect of level setting 2 for factor A is determined by taking the average of experiments 5, 6, 7 and 8. The impact of all the other factor settings can be calculated in a similar manner and the results plotted as illustrated later.

Expt	Control Factor Setting						
No	A	B	C	D	E	F	G
1	1	1	1	1	1	1	1
2	1	1	1	2	2	2	2
3	1	2	2	1	1	2	2
4	1	2	2	2	2	1	1
5	2	1	2	1	2	1	2
6	2	1	2	2	1	2	1
7	2	2	1	1	2	2	1
8	2	2	1	2	1	1	2

Table 1: Table 1. A $L_8(2_7)$ orthogonal array.

3. Implant Monitor

In order to confirm the correct functioning of the implanters, test wafers are processed at specified intervals. The process consists of growing an oxide, performing the implant followed by an anneal, after which, the sheet resistance is measured. To speed up the monitoring cycle time the anneal process was changed from a conventional furnace to an RTA system. At the same time the variation in sheet resistance was observed to increase and this was initially attributed to oxide thickness variation. This was of obvious concern because it reduced the effectiveness of the monitor for identifying potential implant problems.

SUPREM-3 was used to simulate the process described above and an $L_8(2_7)$ orthogonal array used to examine the effect of varying what were thought to be the key control factors. The effect of all these factors on the final sheet resistance is shown in figure 1.

As expected these results show that the oxide thickness does influence the final sheet resistivity. However, somewhat surprisingly, the same change in oxide thickness has a proportionately larger effect when the RTA system is used. All the other control factors have a roughly similar effect upon the sheet resistance except for the dose where the RTA wafers appear to be less sensitive to dose variation.

These results suggest that the perceived problem of oxide thickness variation is not in fact the case. The move to an RTA anneal has made the monitor wafers more sensitive to any changes in oxide thickness, whereas previously, variations of this magnitude did not have any significant effect. Of equal concern is that the RTA wafers were less sensitive to dose variations and hence the monitor, when RTA processed, is less effective. The complete process of designing the "experiment", performing the simulations and processing the results was performed in a single afternoon. This compared with the cost of processing up to 24 wafers with its typical one week cycle time.

4. Depletion Threshold Variation

As part of the continual improvement programme the variation of depletion threshold voltage for the 4μm nMOS products was targeted. This work commenced before

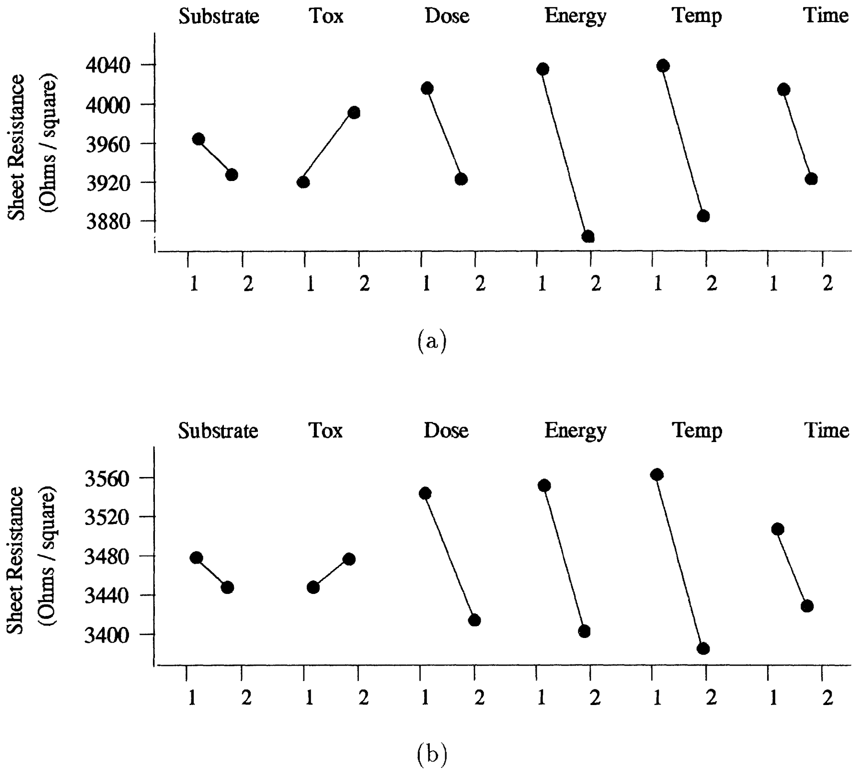

Figure 1: The effect of control factors upon sheet resistivity. (a) RTA, (b) Furnace.

simulation was available on site and so an experiment was run using Taguchi techniques to identify the main controlling factors. A $L_{16}(2_{15})$ experiment, consisting of 16 runs, was performed using 48 wafers. The time taken to run this experiment from the initial design through processing and final analysis was approximately 4 months.

At about the time that final measurements were being performed simulation facilities became available and the experiment was repeated using SUPREM-3. Two days was spent building the data file for the complete nMOS process including de-bugging and characterisation. The various runs as defined by the $L_{16}(2_{15})$ Taguchi array were subsequently modelled on a workstation within 3 hours and the results are displayed in figure 2.

The results obtained from this simulation identified the same controlling factors (and their relative significance) as those identified by the previous silicon experiment. As expected, depletion dose and gate oxide thickness were the most significant factors. However, the exercise also highlighted that the normal variations in wafer substrate resistivity significantly influenced the threshold voltage and this had not been previously considered an issue.

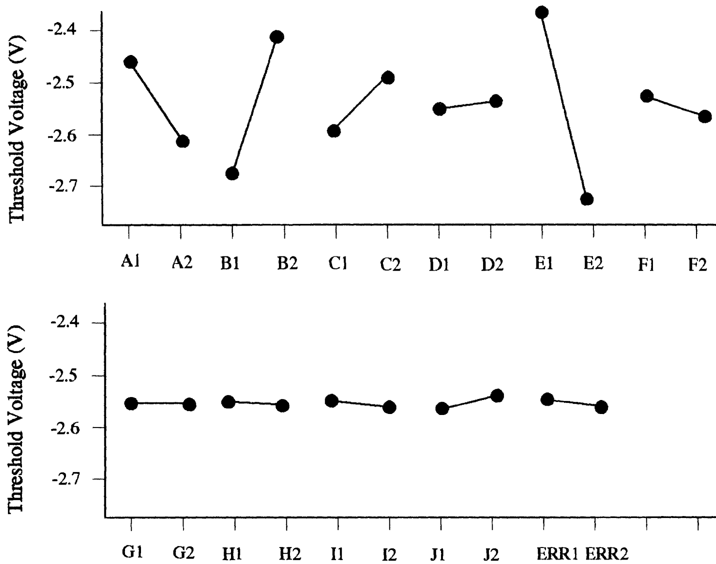

Figure 2: The effect of control factors upon depletion threshold voltage. (A: Wafer Resistivity, B: Gate Oxide Thickness, C: Gate Implant Dose, D: Gate Implant Energy, E: Depletion Implant Dose, F: Depletion Implant Energy, G: Poly Dope Time, H: Arsenic Drive-in Time, I: PSG Reflow Time, J: Enhancement Anneal Time)

5. Conclusions

It has been shown that process simulation can be effectively employed in a large MOS production facility to solve problems. In addition it has been demonstrated that the combination of experimental design and simulation is extremely powerful and can significantly reduce the number of simulation runs required. The two examples detailed above have had significant cost benefits as well as reducing the cycle time involved in the problem solving process.

6. Acknowledgements

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