SIMULATION OF SEMICONDUCTOR DEVICES AND PROCESSES Vol. 5
Edited by S. Selberherr, H. Stippel, E. Strasser - September 1993

Applied TCAD in Mega-Bits Memory Design

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Abstract

This paper describes a methodology of TCAD application in VLSI design and development. Simulation–based circuit model parameter generation for chip design purpose is one of the key topics in TCAD. Several critical phenomena, such as CMOS latchup etc., were also analyzed to verify feasibility and performance of the memory process. Two months of TCAD analysis were required, in which twelve sets of MOS model parameters were generated by VISTA with the computational cost of six hours on six CPUs of SGI-IRIS machines.

1. Basic Data for TCAD Design

For submicron devices, the shallow junction formation is one of the essential processes which determine the device performance. To verify the impurity profile of ion–implanted and annealed diffusion layer, we used SIMS measurement for B, P, and As impurities. Over a hundred samples with various doping conditions have been analyzed. Enhanced diffusion model parameters with annealing temperature and dose have been extracted. Figure 1 shows an example of a Phosphorous implantation/diffusion profile which exhibits dose dependent TED (Transient Enhanced Diffusion) phenomena [1]. The two–dimensional profile of the Phosphorous diffusion was also verified as shown in Fig. 2 [2]. The result shows an isotropic nature of TED for Phosphorous. In circuit design, threshold control and driving current of the device are two major characteristics which determine chip performance and yield. We found an anomalous degradation of submicron MOS driving current based on a study of intrinsic drain current, as shown in Fig. 3 [3]. A simple model which describes carrier–velocity–saturation has been developed to clarify the phenomena. Experimental $I_{ds} - L$ curves in submicron NMOS and the proposed model allow us prediction of effective drain current of submicron NMOS as shown in Fig. 4.

2. Analysis of Critical Phenomena

In CMOS memory process, a couple of critical phenomena have to be evaluated. Simulation works on CMOS latchup immunity [4], memory cell alpha–particle induced soft error [5], Si crystal defects formation due to LOCOS process related mechanical stress [6] and electric–field enhanced SRH recombination [7] have been conducted.

Qualitative (semi-quantitative) studies predicted a relative process margin with help of extensive experimental data in conventional processes. One example of the analysis is the CMOS latchup immunity being enhanced in shallow wells with retrograde structure, as shown in Fig. 5.

3. Generation of Circuit Model Parameters

In VLSI memory development, concurrent engineering, i.e. simultaneous work on chip/circuit design and fabrication process does appear in many cases. Our TCAD methodology to meet this needs is shown below:

1. Initial process debugging by 2D process analysis
   When the process designer proposed the initial process flow, fabrication steps have been analyzed using 2D process simulators with calibrated parameters (cf. Section 1) with a focus on ion implantation and annealing. A couple of mis-settings in impurity dose were found by simulation. Also optimum conditions in ion implantation dose and energy were determined by the initial TCAD verification.
2. Worst-case device definitions
   In circuit design, worst case analysis has been used to ensure operation even in the worst process variation extreme. In our case, gate length definition, gate-oxide thickness variation, and channel dose variation were chosen as process variations to be considered in circuit simulation. Based on this design strategy, $I-V$ characteristics of six device structures for both N&PMOS, have been defined for circuit design and analysis.
3. Generation of $I-V$ data
   The TCAD system VISTA [8] conducts 2D process/device simulations for the twelve devices of N&PMOS's. Computed I_{ds} data in bias conditions of V_{bb}, V_{gs} and V_{ds} are arranged into a pre-determined format for parameter extraction. Six hours in CPU time were required to compute twelve sets of $I-V$ data (2448 bias points total) on six SGI-IRIS CPUs in parallel.
4. Calibration of generated $I-V$ data
   Since some simulation models are assumed to remain uncertain as well as unknown process variations in fabrication line, an experimental $I_{ds}-L$ curve of a similar submicron NMOS (see Section 1) is used to calibrate the generated $I-V$ data. A simple I_{ds} normalization (scaling) at maximum drain current proved to be accurate for submicron NMOS as shown in Fig. 6.
5. MOS model parameter extraction
   The calibrated $I-V$ data are formatted as input deck for the MOS model [9] parameter extraction program. Four examples of the extracted MOS model are shown in Fig. 7. The averaged RMS error of the twelve devices obtained in this work is less than 1%.

4. Conclusions

A TCAD application in VLSI memory design has been conducted. Simulation-based circuit model parameter generation for chip design purposes was performed based on a TCAD database. Critical phenomena such as CMOS latchup were analyzed to verify feasibility and performance of the memory process. Two months of TCAD analysis were required, in which twelve sets of MOS model parameters were generated by VISTA with the computational cost of six hours on six CPUs of SGI-IRIS machines.

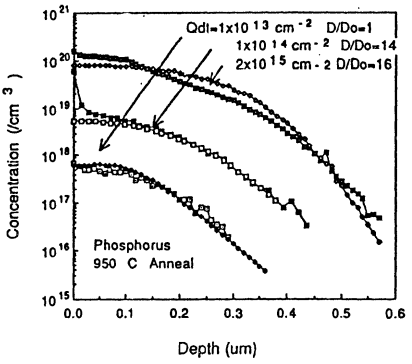

Fig.1 Determination of Phosphorous Implant./diffusion parameters at 950C furnes annealing.

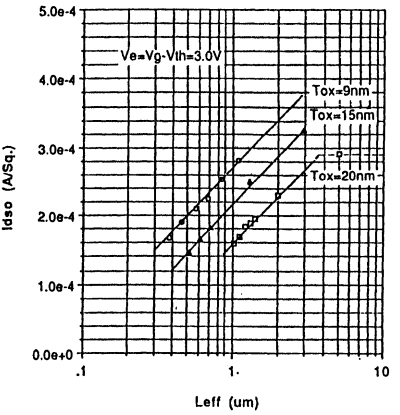

Fig. 3 Anomalous degradation of drain current (of unit area: W/L=1) found in submicron NMOS measurements.

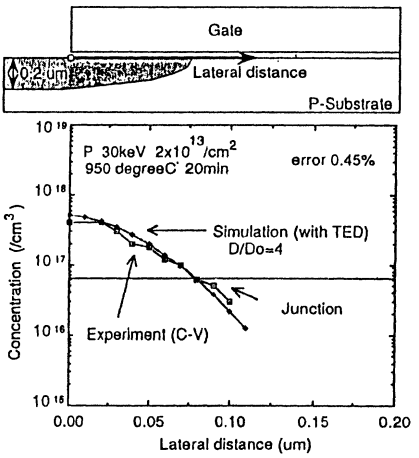

Fig.2 Experimental verification of 2D diffusion of phosphorous with TED (Transient Enhanced Diffusion) effects.

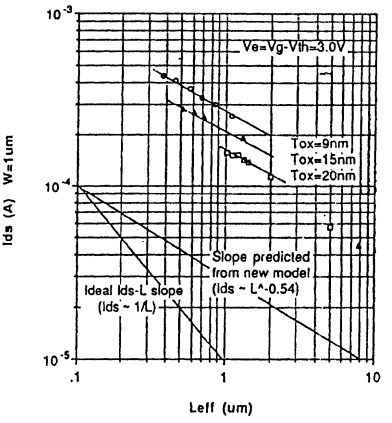

Fig.4 Empirical Ids-L curves and comparison with proposed model which describes velocity-saturation effect.

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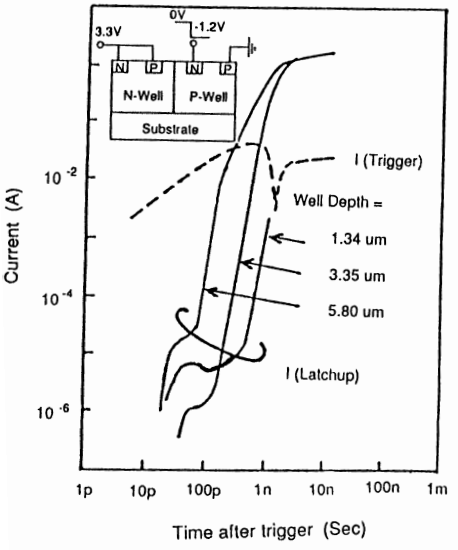

Fig.5 2D latchup simulation as a parameter of depth profiles in N- & P-wells.

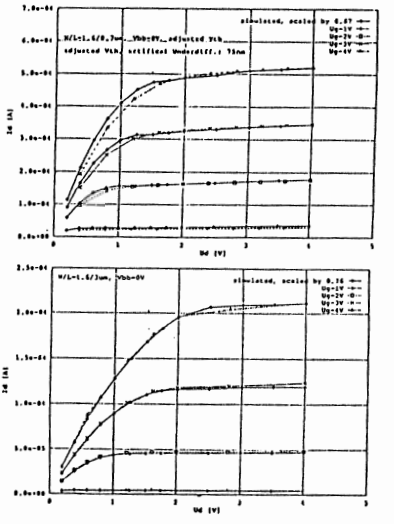

Fig.6 Evaluations of scaling technique to adjust simulated Id-Vd curves to experimental one. (dashed: experiments, solid: simulated & scaled)

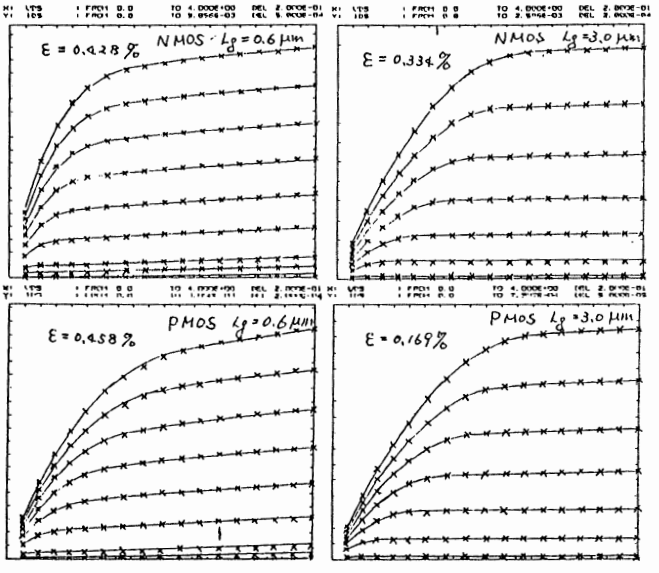

Fig. 7 Circuit MOS models for 0.6um and 3.0um N & PMOS's, that are generated using I-V process/device analysis and automatic parameter extraction.
(symbol: simulated & scaled data, solid line: models)