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Quasi Two-Dimensional Numerical Simulation of SiGe/Si MOSFETs

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Abstract

Results of the charge distribution and terminal behaviour of Si/SiGe/Si p-channel devices are presented for various gate voltages and device geometries. The results are based on a quasi two-dimensional numerical model where Poisson's equation is solved for the electric potential in the longitudinal direction with the subsequent lateral current transport obtained using an integral method.

1. Introduction

The differing lattice constants between the epitaxially grown SiGe alloy and the underlying Si substrate leads to an inherent strain in the alloy which significantly enhances the optical and electronic properties of the material [1]. The in-plane compressive stress in the $Si_{1-x}Ge_x$ layer results in a considerable reduction of the energy gap [2] making the alloy very attractive for the fabrication of high performance transistors and optoelectronic devices. This includes heterojunction bipolar transistors [3], MODFETs [4], and photodetectors for 1.3 μm wavelength [5].

More recently, there has been growing interest on SiGe MOSFETs for purposes of achieving higher performance p-channel transistors [6]. They are based on the Si/SiGe/Si structure where the active region is within the SiGe layer which is separated from the gate oxide by a thin cap (or spacer) layer. These devices have the advantage of higher hole mobilities [7] and furthermore, they do not suffer from mobility degradation due to surface scattering. However, one main problem that still remains with these devices is the gate-induced inversion layer at the oxide/Si interface which reduces the performance at moderate gate bias.

In this paper, we present modelling results of charge distribution and current-voltage characteristics of p-channel Si/SiGe/Si MOSFETs based on a quasi 2-D model. At very low gate voltages, conduction predominantly takes place in the SiGe layer where the hole mobility is inherently higher thus enhancing the device transconductance. However, with increasing gate bias, an inversion layer is induced at the oxide/Si interface; the conduction cross over point occurs at a lower gate voltage for larger cap layer thickness.

2. Modeling Equations

The device cross section and corresponding energy band diagram is shown in Fig. 1. The device comprises of a strained n-SiGe layer pseudomorphically grown on a (001) n-Si substrate followed by a n-Si cap (or spacer) layer passivated by a low temperature oxide. With a negative potential on the gate electrode, the valence band moves upwards causing an accumulation of holes at the Si/SiGe interface (see Fig. 1). With further increase in the gate voltage, a hole inversion layer is created at the oxide/Si interface. Assuming that the electron Fermi potential is uniform from the bulk to the oxide/Si interface, and the hole Fermi potential is displaced by the applied voltage V, the longitudinal potential distribution is obtained by solving Poisson's equation [8],

$$d^2\psi/dx^2 = -(q/\varepsilon_s)\,[(p_{no}e^{q(V-\psi)/kT} - 1) - (n_{no}e^{q\psi/kT} - 1)]. \tag{1}$$

in one-dimension. Here, Boltzmann's statistics is assumed for the mobile charge density. In (1), ε_s denotes the semiconductor permittivity, and n_{no} and p_{no} are the equilibrium densities of electrons and holes, respectively. The majority carrier concentration, n_{no} is taken to be equal to $N_D \sim 10^{16}\,cm^{-3}$ for all regions. The minority carrier concentration, p_{no} is given by n_{ie}^2/n_{no}, where n_{ie} is the intrinsic carrier concentration which is position-dependent due to bandgap variations. The resulting p_{no} may lead to error in view of possible discontinuity in the conduction band. But the discontinuity is significantly smaller than ΔE_v and hence the relative error is expected to be small. The intrinsic carrier concentration in the SiGe layer is modelled as

$$n_{ie,SiGe} = (n_{ie,Si}/f_c f_v)\exp[q\Delta E_v/2kT], \tag{2}$$

where $n_{ie,Si}$ is the effective intrinsic concentration in Si, f_c accounts for the strained induced energy shifts in the conduction band and f_v takes into account the strained induced distortions and sub-band splitting in the valence band. For 30% Ge fraction, their values are $\sqrt{(3/2)}$ and 2, respectively (see [9] and references therein).

Equation (1) is solved within the semiconductor regions subject to the following boundary conditions. Deep in the substrate, the electric potential is assumed zero. At the oxide/Si interface, the potential is prescribed by

$$\psi_s = V_G - t_{ox}\,(d\psi/dn), \tag{3}$$

where V_G denotes the gate voltage, t_{ox} is thickness of the oxide, and n is normal to the interface. The discretization of (1) was based on a finite difference scheme. The permittivity was assumed to be uniform; the variation in the permittivity due to Ge content was small and its effect on the potential distribution is negligible. The oxide thickness was assumed to be 100 Å. The solution to eqns. (1)-(3) yield the electric potential which is tabularized for various voltages V, to be used in subsequent numerical computations of the charge distribution and terminal behaviour, viz.,

$$Q_{p,Si} = q\,p_{no}\int_{\ell_{Si}} e^{q(V-\psi)/kT}\,dx \tag{4}$$

$$Q_{p,SiGe} = q\,p_{no}\int_{\ell_{SiGe}} e^{q(V-\psi)/kT}\,dx \tag{5}$$

$$I_{DS} = (qW/L)\int_{V_{DS}}\left[\int_{\ell}\mu_p\,p_{no}\,e^{q(V-\psi)/kT}\,dx\right]dV. \tag{6}$$

Here, ℓ_{Si} and ℓ_{SiGe} denote the thickness of the Si and SiGe layers, respectively, and ℓ being the total layer thickness, and μ_p is the hole mobility which is taken to be electric field dependent.

3. Results and Discussion

The hole charge concentration at the oxide/Si interface, $Q_{p,Si}$ and Si/SiGe interface $Q_{p,SiGe}$, computed for various gate voltages is illustrated in Fig. 2 for two spacer layer thicknesses. The charge $Q_{p,SiGe}$ is seen to be larger than that of $Q_{p,Si}$ only at small gate voltages, $|V_G|$. As the gate voltage is increased, the inversion layer charge starts to predominate; the behaviour being consistent with experimental observations reported in [6]. The conduction cross over point, at which the charge in the Si and SiGe layers

become equal, occurs for low values of $|V_G|$ for thicker spacer layers (see Fig. 3). The thickness of capping layer used is 10.8 nm. The dependence of drain current on gate voltage is illustrated in Fig. 4 for the SiGe MOSFET and an equivalent surface inversion MOSFET serving as a control. Also shown are the measured results of Garone *et al.* [10]. The SiGe MOSFET clearly exhibits enhanced transconductance due to the higher hole mobility in the strained layer as well as due to reduced surface scattering. The discrepancy between simulations and measurement results [10] at low $|V_G|$, where conduction predominantly takes place at the Si/SiGe interface, can be attributed to the possible presence of dislocations at the interface which cause the mobility to decrease due to additional scattering. The simulated current-voltage characteristics or both devices is shown in Fig. 5 for different gate voltages. Despite the high concentration of surface layer charge, the contribution of the higher mobility inversion layer charge at the Si/SiGe interface is significant thus yielding enhanced terminal behaviour.

4. Conclusions

In this paper, we have presented the charge distribution at the oxide/Si and Si/SiGe interfaces for various gate voltages and cap layer thickness. A significantly enhanced performance has been obtained with the SiGe MOSFET due to the high hole mobility in the strained layer and due to reduced surface scattering.

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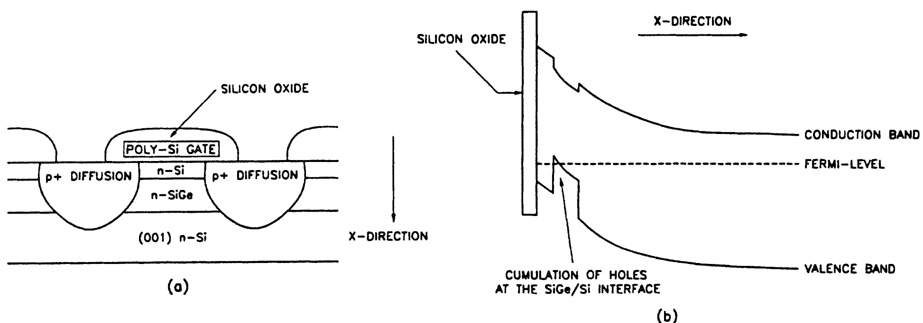

Figure 1: (a) Cross section of SiGe MOSFET and (b) its band structure.

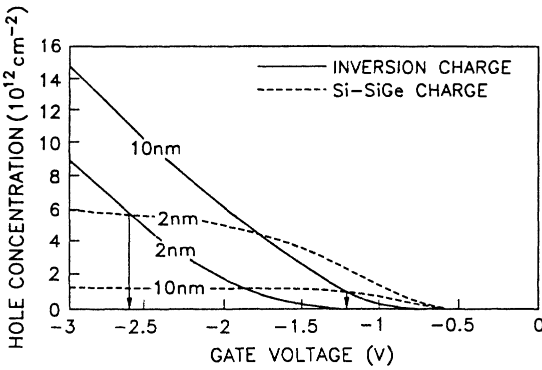

Figure 2: The oxide/Si and Si/SiGe inversion layer charge density as a function of gate voltage for different spacer layers. The vertical arrows denote cross over points, $Q_{p,Si} = Q_{p,SiGe}$.

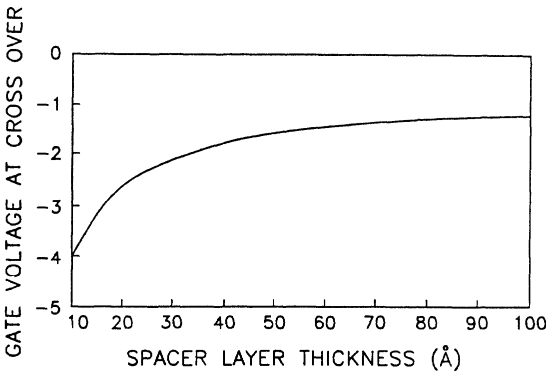

Figure 3: The gate voltage at which cross over occurs as a function of spacer layer thickness.

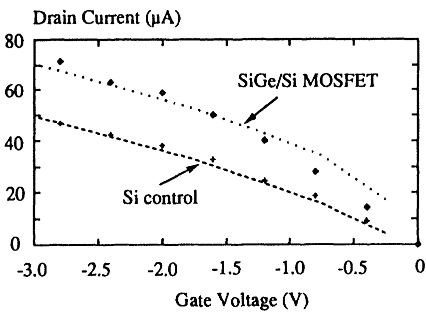

Figure 4: The drain current as a function of gate voltage for a SiGe MOSFET and a Si control device. $V_{DS} = 0.2$ V.

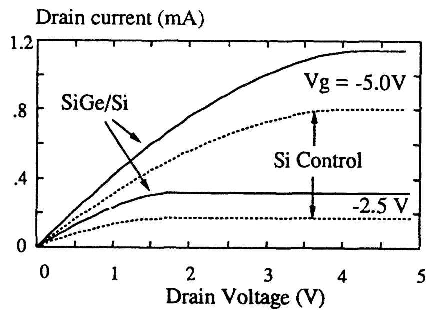

Figure 5: I-V characteristics of the SiGe and Si-control MOSFET devices.