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Coupling a Statistical Process-Device Simulator with a Circuit Layout Extractor for a Realistic Circuit Simulation of VLSI Circuits

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Abstract

This paper discusses methodology of statistical simulation of an IC design which includes disturbances described by independent random variables, spatially correlated random disturbances and deterministic process parameters distribution on a wafer. The method of coupling of a process/device simulator with a circuit extractor is proposed. Practical example of an operational amplifier design optimization is presented.

1. Introduction

The performance and parametric yield of integrated circuits often suffer from process-related variations of parameters of IC components. Ordinary simulation tools are not sufficient to predict the IC performance when process-related parameter variations are of primary concern. A method of statistical simulation has been proposed [1] which accounts for random global and independent local variations of process parameters in a hierarchical way [2]. A statistical process/device simulator implementing this simple model of process-related variations [3] can provide good approximation for the variations of parameters of single devices. If statistical process/device simulation is coupled with circuit simulation, useful statistical information can be obtained for circuits which are not very sensitive to local variations of device parameters. However, experience [4, 5] shows that for precise analog circuits and for large digital VLSI chips spatial dependencies of deterministic variations and correlations of random variations cannot be ignored. For realistic statistical simulation a more complex model of process-related variations is necessary. Such a model should be able to handle: (i) global variations, (ii) local variations described by deterministic functions of device position on the wafer, (iii) local variations described by independent random variables, and (iv) local variations described by spatially dependent random variables. In this work we propose a methodology of statistical simulation which accounts for such variations and describe practical implementation of this methodology.

2. The problem of coupling CAD tools

The basic idea of statistical process/device/circuit simulation is to couple four tools: a process simulator, a device simulator, a circuit extractor and a circuit simulator, and use them in a Monte Carlo loop. However, in practice coupling an extractor with a process and device simulator is not straightforward. If local variations and their spatial dependencies are to be accounted for, the process simulation should be performed separately for every component before device simulation. Moreover, the circuit netlist and all the geometrical information (i.e. locations, shapes and sizes of the components) have to be extracted from the layout by a circuit extractor and passed to the device simulator. This requires an enormous amount of data to be transferred from process simulator and from extractor to device simulator (e.g. descriptions of all the shapes and one- or two-dimensional doping profiles at hundreds of locations). To avoid this we split the device simulation task into two: modeling of passive components is performed within the circuit extractor and the rest of the device modeling is integrated with process simulation. More precisely, we base our solution on the following assumptions:

Assumption 1. For the purpose of this work all the components can be divided into two classes: *process-dependent components* and *geometry-dependent components*. The first class includes components which are geometrically simple but whose parameters depend on fine details of the results of the manufacturing process. A good example is a MOS transistor. Its parameters depend strongly on the doping profiles in the channel and source/drain regions but the mask geometry can be described by just two numbers: channel width and length. The second class includes components of complex geometry but simple dependence on the manufacturing process. An example is parasitic resistance of a polysilicon region of complex shape. Its dependence on processing parameters can be characterized by a single number - the sheet resistance. To minimize the data flow between the simulation tools, it is convenient to combine the modeling of process-dependent components with the process simulation and modeling of geometry-dependent components with circuit extraction.

Assumption 2. Performance of well designed integrated circuits may depend critically on *local* variations and spatial dependencies of parameters of a set of components called *critical components*, but not on *local* variations of parameters of *parasitic* passive components. In a general case the set of critical components may include active devices and possibly some passive components, e.g. capacitors in a SC filter, but in current implementation MOS transistors are the only critical components available. We assume that all critical components are sufficiently small so that all the physical parameters such as oxide thickness, doping, resistivity etc. can be considered uniform within the component area.

These assumptions allow to organize the simulation in the way shown in Fig. 1.

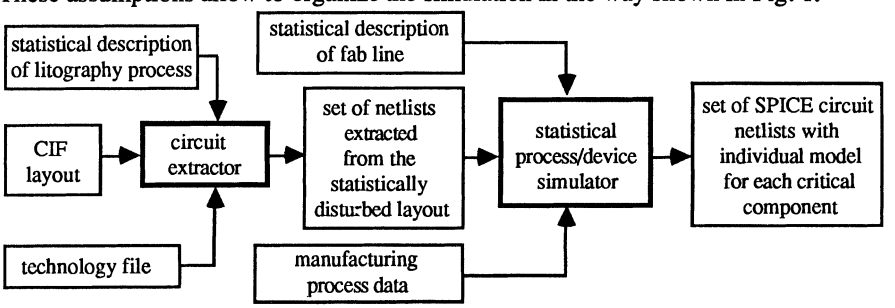


Fig.1. Generation of a set of netlists representing circuits affected by process variations and layout disturbances.

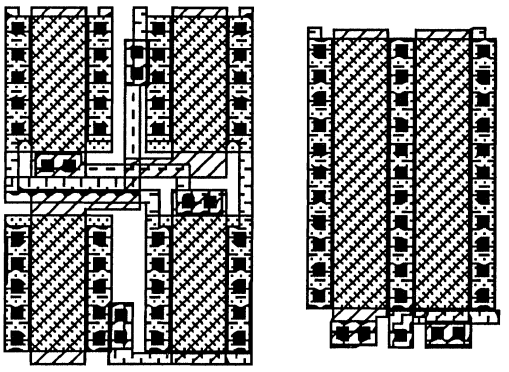
First, the extractor simulates layout disturbances and performs extraction creating a netlist which also includes the (x,y) coordinates of all the critical components. Then the process and device simulator adds a separate device model for each critical component on the netlist. To generate these models, full process simulation and device modeling is repeated for every critical component, and the positions of components are taken into account when disturbed process parameters are generated. The outcome of modeling is a data file for a circuit simulator. Such file enables for electrical simulation which accounts for local and global process parameter variations and lithography related disturbances for all critical components. Having such a statistical sample of netlists one can make a number of circuit simulations and estimate the range of values for electrical parameters of the design (e.g. delay time, input offset voltage, gain, slew-rate, linearity).

3. Special features of the programs

To implement the methodology described above, we developed two programs: EXCESS II - a layout extractor which can handle layouts with lithography-related deformations, and SYPRUS - a statistical process/device simulator which combines numerical efficiency with accuracy of process simulation and MOS device modeling. Both programs can simulate global random variations, local uncorrelated variations, local spatially correlated variations and wafer-wide deterministic distribution of process parameters and layout geometry. The circuit extractor EXCESS II [6] takes a CIF file as input, uses appropriate technology data to simulate layout deformations and then carries out circuit extraction. The extractor can process shapes described by polygons with arbitrary angles what is important if one wants to extract a circuit from the layout affected by arbitrary deformations. The device modeling in EXCESS II includes computations of W/L ratios for the transistors with process-disturbed geometry as well as modeling of RC parasitic devices [7]. The output consists of a set of netlists representing a sample of fabricated chips. Each netlist contains information about global coordinates of each critical component within the wafer. The process/device simulator SYPRUS generates disturbed process parameters and performs the process simulation and device modeling for each critical device from each netlist (e.g. a SPICE model for each MOS transistor) and outputs the netlist in SPICE format. All important geometrical dependencies such as dependence of threshold voltage on transistor channel length are taken into account. As a result, a set of netlists is produced which includes devices with models corresponding to variations of such parameters as etching rate, mask alignment, oxidation time, temperatures etc.

4. Example: optimization of an operational amplifier design

An example of application of our approach is shown in fig. 2. The sensitivity of input offset voltage of a CMOS operational amplifier to the layout of the input stage was investigated. Since the amplifier was to be used as a building block in an artificial neural network chip, the goal was to make the whole design as compact as possible while maintaining low offset input voltage. Two versions of input stage layout were considered: the common centroid layout (Fig.2a) and the simple layout (Fig. 2b). The process data were typical for an industrial n-well CMOS process. All types of variations were included. The positions of simulated circuits are shown in Fig.3. The results of simulation for 180 simulated circuits were as follows. For both layouts the mean value of the input offset voltage was almost the same (0.037 mV), but for the common centroid layout the standard deviation was 3.2 mV while for the simple layout the standard deviation was significantly larger: 5.0 mV. As expected, the common centroid layout yields smaller input offset voltage due to partial compensation of local variations. These results may help to decide whether for a particular application the input offset voltage of the simple layout is acceptable or the common centroid layout must be used.



a) b)

Fig. 2. Two versions of input stage of a CMOS operational amplifier

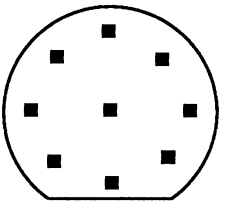


Fig. 3. Positions of simulated circuits on a wafer

5. Conclusions

For realistic prediction of performance and yield of integrated circuits sensitive to local variations of process parameters and layout disturbances it is necessary to include spatial dependencies of these variations. A method of coupling of circuit extractor with process/device simulator and circuit simulator has been proposed. Special properties of the programs and the method of coupling allow to include spatial dependencies of process variations in the statistical simulation of the circuit's behavior. An example shows how such a simulation may help to find an optimal design when there is a tradeoff between circuit size and performance.

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