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Predicting Manufacturing Variabilities for Deep Submicron Technologies: Integration of Process, Device, and Statistical Simulations

Z. Krivokapic and W. D. Heavlin

Advanced Micro Device
P.O. Box 3453, Sunnyvale, CA 94088, USA

Abstract

Process and device simulators are used to project the long term manufacturing distributions of 0.35 μm, planarized, concave transistors. Particular care is taken to calibrate the simulators, and to quantify the contribution from each manufacturing source of variation.

1. Introduction

To introduce a new integrated circuit technology efficiently, the performance characteristics and manufacturing specifications must be determined as early as possible. This allows circuit design to proceed in parallel with technology development, and manufacturing hardware to be chosen appropriately. A major limitation to technology development is the complexity of the technologies themselves, and their correspondingly slow manufacturing cycle times. Process and device simulators, well calibrated, promise some relief, by allowing us to test simple theories more easily, to consider more alternatives than silicon, and to determine optimum targets.

In this paper, we extend the application of such simulators to project the long term manufacturing distributions of transistor parameters[1,2]; our example is a 0.35 μm planarized and concave device, for which we are able to make predictions before achieving first silicon. Our approach features minimum silicon, TSuprem4 and Medici process and device simulations, an objective calibration method, and some adapted statistical methods. We estimate not only the long term total manufacturing variation, but also decompose it into components associated with different manufacturing steps. By knowing the total expected manufacturing distribution, we can design circuits to be more robust. By quantifying the components of this distribution, we can determine process performance objectives and select equipment more appropriately.

2. Technology

The device is a 0.35 μm self-aligned channel transistor(Fig. 1). Note that it is fully planarized and concave. LDD diffusion comes from a doped polysilicon layer. Since the gate area is etched through the oxide layer, the damaged underlying silicon has to be removed; once removed, a trench in the silicon results.

By selectively limiting threshold adjust and punchthrough stop implants to the channel region only, we are able to self-align the channel to the source and drain. This decreases the source/drain resistance, and improves hot carrier immunity.

3. Method

Our method consists of five distinct steps: (a) Using an earlier generation technology, we run simulations over a broad range of possible factors, in order to identify those parameters with the most influence on device performance. (b) In silicon, we design and execute a factorial experiment varying these parameters.

(c) We complement the splits of the silicon experiment with simulations. Wherever feasible, two-dimensional device simulations are used. In the case of the p-channel device, sidewall leakage current along the trench isolation requires that we use the three-dimensional simulator DaVinci[3].

By correlating silicon and simulation results, we define a calibration relationship for subsequent simulations, broadly valid over a range of parameter values. This calibration approach is to be distinguished from the usual industry calibration practice, which fits limited experimental data - often just one device - by changing selected parameters in the process and device simulators. In our case, our experimental data is from a factorial lot with a deliberately broad range of process variations, not directly amenable to the usual approach. Further, uncontrollable, unmeasurable variations from contamination, plasma damage, and mechanical stress can effect device characteristics dramatically, yet with present-day tools we are not able to simulate them. Finally, critical dimension control is not fully mature for sub-half-micron devices, and we need to compare devices with the same effective channel lengths.

For all these complications, our calibration approach is straightforward. All process and device simulations use only default parameter values. Simulations of devices at nominal dimensions are compared to the corresponding structures in silicon - without taking into account effective channel lengths. These are compared in scatterplots, such as in Fig. 2. For each scatterplot, we calculate the linear relationship by least squares. This allows us to transform all simulated results into predictions of what is most likely to occur in silicon. In the simulation experiments subsequently described, we use these transformations throughout, always report calibrated values, and make no further reference to calibration.

(d) Following a Latin hypercube design[4], we characterize the non-linearities of the parameter space with additional simulations. The "noise factors" are those parameters most difficult to control in manufacturing, and most likely to induce substantial variation in device performance. For our device, four of the noise factors (ranges) are gate oxide thickness (8.5 and 9.5 nm), gate length, gate trench depth (50 and 100 nm), and spacer width (30 and 50 nm). A fifth noise factor, the source and drain resistance, is a combination of doping, critical dimension, and mask registration error variation.

(e) From these simulations, we predict the distributions of the device's current and voltage characteristics. Using a multivariate interpolator[5] we estimate the improvement in distribution that results from perfect control of each noise factor singly, that is, the amount of manufacturing variation each factor induces.

4. Results

Our example assesses a technology in an early stage. We conclude from Table 1 that n-channel V_t's are most affected by gate oxide thickness variation, linear transconductance by gate critical dimensions, drive current and large signal transconductance by gate trench depth variations, yet can be controlled sufficiently.

In the case of p-channel devices, the blanket punchthrough stop implant, not selective to the channel region only, causes problems. As shown in Table 2, the control of threshold voltage, linear transconductance, and drain-source current are of the order of 10 percent one-sigma. Further, any variation in gate trench depth drastically affects device characteristics. We conclude that to ensure manufacturability one must use either a self-aligned punchthrough stop implant, or drastically improve trench depth control.

5. Summary

Any methodology evaluating manufacturability must be objective and reproducible. Our approach fulfills is so in several ways: The simulations are grounded in silicon over a manufacturing window, robust to any single observation, yet based on default parameters. As a result, our calibration approach is easily automated, reproduced, and commercialized. In the analysis, the percent of variation each factor contributes to the total is quantified, complementing the projected distributions.

6. References

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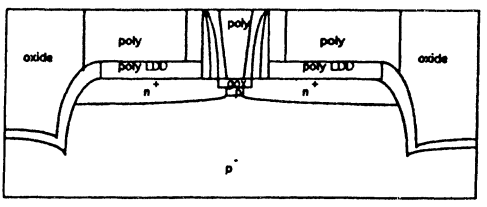

Fig. 1: Cross-sectional view of an n-channel concave device with recessed gate oxide and selectively implanted channel region.

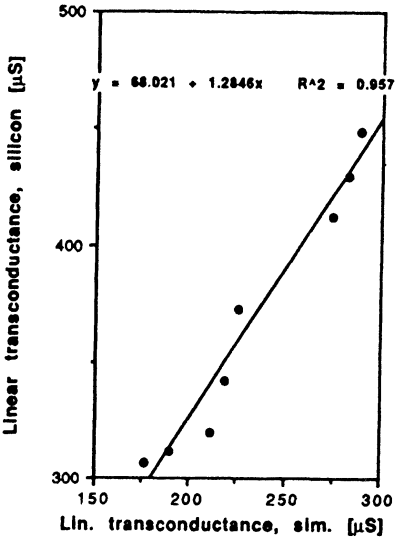

Fig. 2 (on the right): Calibration curve for linear transconductance for 0.5 μm concave devices.

N-Channel Analysis of Manufacturing Variation

	V_t	g_m	g_{ds}	I_{ds}
typical	0.43 V	31.1 μS/μm	377 μS/μm	793 μA/μm
one sigma	0.014 V	2.17	20.2	61.1
L_s	12.66 %	7.16 %	19.46 %	21.48 %
L_o	0.95	13.43	11.18	14.39
L	25.26	44.93	17.59	24.07
T_{ox}	57.15	11.93	1.99	3.13
W_{ox}	11.67	1.97	0.03	5.12
D_C	-2.11	22.34	44.29	34.27
interactions	5.56 %	1.76 %	-5.47 %	2.46 %

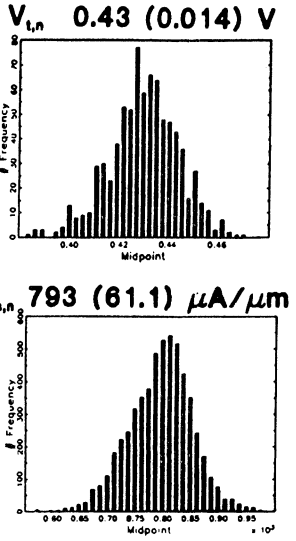

Fig. 3, 4, and Table 1: Simulated n-channel distributions for I_{ds} and V_t, and analysis of manufacturing variation.

P-Channel Analysis of Manufacturing Variation

	V_t	g_m	g_{ds}	I_{ds}
typical	-0.516 V	9.85 μS/μm	108.5 μS/μm	-313 μA/μm
one sigma	0.0475	1.31	2.16	44.6
L_s	-5.78 %	3.19 %	-3.55 %	-3.30 %
L_o	1.01	-4.69	10.46	1.01
L	32.43	38.09	52.46	42.35
T_{ox}	13.52	9.80	16.97	3.48
W_{ox}	-0.33	3.70	-5.25	-2.92
D_C	57.81	53.67	55.95	57.08
interactions	-1.34 %	3.76 %	27.04 %	-2.30 %

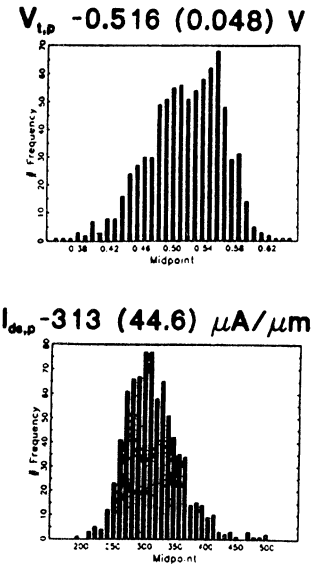

Fig. 5, 6, and Table 2: Simulated p-channel distributions for I_{ds} and V_t, and analysis of manufacturing variation.