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3D Thermal/Electrical Simulation of Breakdown in a BJT Using a Circuit Simulator and a Layout-to-Circuit Extraction Tool

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Abstract

A method for the generation of circuit models for fast thermal-electrical simulation of 3D device structures with a circuit simulator is proposed. It has been used for simulation of the influence of layout parameters on the Safe Operating Area of a BJT and to study the mechanisms that start breakdown processes. For a thermally instable switch-on behaviour of a BJT, a comparison with measurements has been made.

1. Introduction

In this paper we present a tool for 3D thermal-electrical simulation of devices using a circuit simulator. It can be used by circuit designers for optimizing the thermal-electrical characteristics of (power) devices by modifying layout parameters. Coupled thermal-electrical circuits are generated by a layout-to-circuit extractor using a device description based on the layout and the technology used [1]. A comparison with measurement results is done for thermal runaway in a BJT. An application is shown for optimization of the Safe Operating Area (SOA) of a BJT. The advantages of this simulation method compared to the alternative, thermal-electrical device simulation [2] (using the semiconductor transport equations), are discussed. Besides device optimization, this simulation method is used to obtain insight in the coupled thermal-electrical mechanisms that lead to thermal instability and breakdown.

2. Simulation method and circuit generation

The method for simulation of thermal-electrical device behaviour with a circuit simulator has been described in [3,4]. Our circuit model generation is based on the device layout (masks), technological process parameters (e.g., sheet resistance), and the chip dimensions. The circuit representing the device is built up with layers. Each layer represents a distinct part of the device (e.g., an emitter region of a BJT), and is built on a lateral triangular mesh with vertical elements located on the nodes (for the connection with other layers), and lateral elements on the edges (connecting nodes in a layer). The layers are defined by using logical functions regarding the mask information and technology description. The latter determines

what type of circuit elements will be generated between the nodes in a layer or as a connection between different layers. Figure 1 shows a BJT built up with layers. For the discretisation two grids are used, one for the area in which the time dependent heat flow equation is solved, and one for the area in which the electrical model equations are solved. The meshes coincide in the area where the coupling between thermal and electrical circuit occurs by means of power dissipation and temperature. The transistor model that has been used in the simulations, is an Ebers-Moll model, extended with avalanche multi-plication and high injection effects [3]. The thermal network consists of resistances and capacitances. The thermal conductance was assumed constant here.

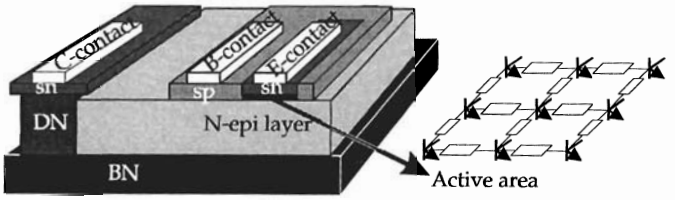

Figure 1: BJT built up with layers. The active area is represented with 9 transistors in this case.

3. Verification, comparison with measurements

The switch-on behaviour of a BJT with five emitters (of 36x100 [μm^2] each) has been used for a comparison of simulation and measurement results. The layout of this structure is shown in figure 2. Only the left half of the structure was simulated because of symmetry. A constant total emitter current I_E=100 [mA] and a constant base-collector voltage V_{BC}=55 [V] were applied at t=0 [s]. The five emitter potentials were all kept at the same level (error < 0.1 [mV]).

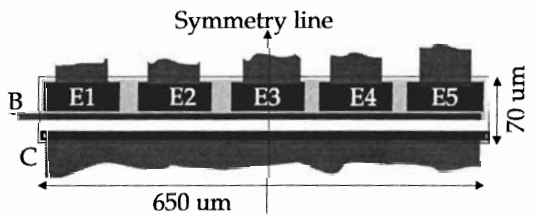

Figure 2: Layout of test structure with 5 emitters.

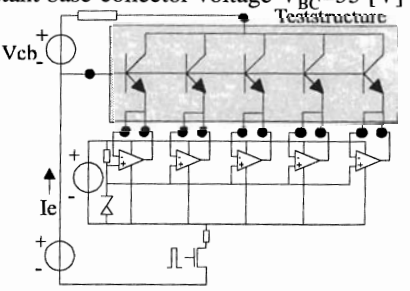

Figure 3: Measurement setup

This was done using a control circuit as shown in figure 3. Because of temperature gradients built up in the device, the current redistributes over the five emitters when time increases. Figure 4 shows the measured and the simulated emitter currents versus time. The measurement results show a difference between the currents of

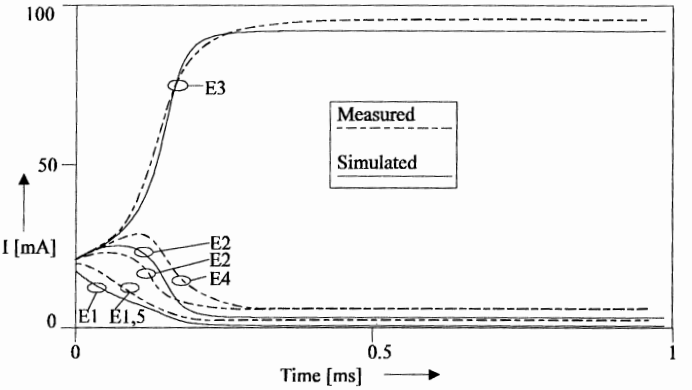

Figure 4: Simulated and measured emitter currents. E1-E5: Emitter 1 to 5.

emitter 2 and 4. This is due to an unintended asymmetry in the device structure (and not because of offset in the control circuit). The central emitter conducts most of the total current after 0.2 ms. A good agreement between measurement and simulation results is obtained. Figure 5 shows the simulated collector current distribution and the temperature distribution in the emitter area after 0.1 and 1 [ms]. The base current crowding effect causes the high current densities at the emitter edges in figure 5A. The effect of the temperature distribution at t=0.1 [ms] (figure 5B) is visible in the current distribution (figure 5A); in y-direction the highest current occurs in the center. The maximum temperature rise in the transistor is about 260 [K] at t=1 [ms] (figure 5D).

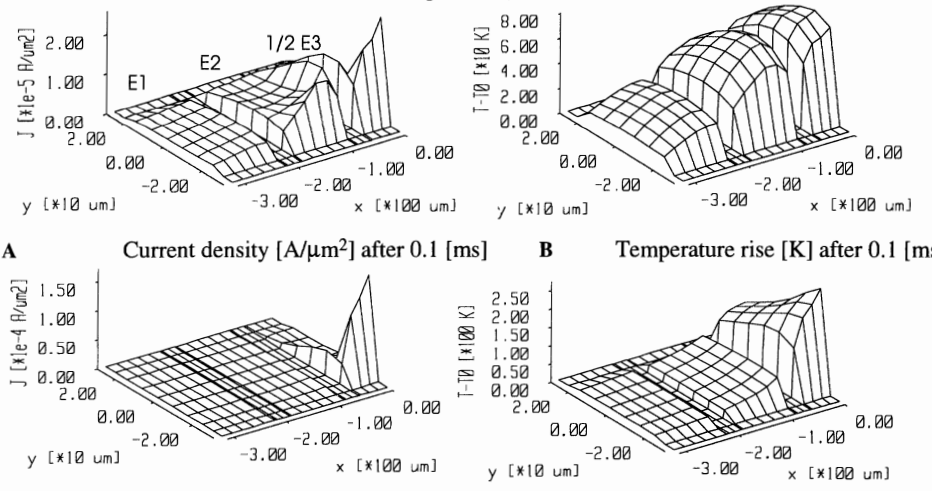

Figure 5: Current (A & C) and temperature (B & D) distribution for t=0.1 [ms] (A & B), and t=1 [ms] (C & D). Note: Only in the emitter areas the data were plotted.

4. Optimization of the SOA of a BJT

In a BJT power dissipation in combination with avalanche multiplication are the major factors determining the boundary of the Safe Operating Area (SOA). Both factors depend strongly on the transistor layout. Therefore a SOA can be optimized using layout modifications. The simulation results demonstrate the influence of an extra base contact and a modification in the emitter contacting on the SOA. Figures 6 and 7 show the layouts and the SOA's of the various transistors respectively.

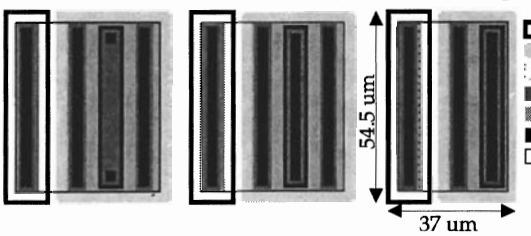

Figure 6: Layouts of simulated BJT's. Left: two small emitter contacts and two base contacts, middle: two base contacts, right: one base contact.

The extra base contact reduces the base resistance. This improves the SOA because it increases the snapback voltage with 4 [V] (10 %) in the high voltage ($V_{CE} > BV_{CE0}$), low current region where avalanche multiplication appears to be the dominant factor for the snapback point. In the high current, low voltage region the base resistance counteracts the positive temperature dependency of the collector current. The base resistance reduction also reduces this compensation, and

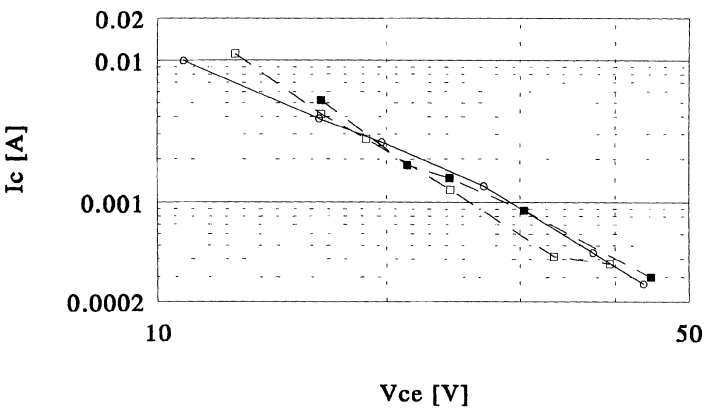

Figure 7: SOA's of simulated BJT's.
■: two small emitter contacts and two base contacts
○: total emitter contacting and two base contacts
□: total emitter contacting and one base contact.

therefore a lower snapback voltage is obtained in this region. The smaller emitter contacts results in a higher emitter series resistance especially for the sections in the middle of an emitter area. In the high current regime the emitter resistance decreases the current in the non contacted emitter area and concentrates it near the contact. This influences the temperature and current distribution and results in a much more uniform temperature distribution along the emitter than in the transistor in which the total emitter area is contacted.

5. Conclusions

The method for 3D thermal-electrical simulation using a circuit simulator and a layout-to-circuit extraction tool has been described and verified with measurements. An application has been shown for optimization of a Safe Operating Area of a BJT. The proposed method has a number of advantages compared to the alternative, 3D thermal-electrical device simulation (using the semiconductor transport equations):

1) It allows circuit designers to simulate the thermal-electrical device characteristics with the circuit simulator they are used to.
2) The cpu-time is orders of magnitude smaller. This makes it suitable for simulation of characteristics with many bias points. The average cpu time necessary for simulation of one bias point of the test structure in section 3 (containing 6925 circuit elements and 2074 nodes) was 125 [s] on an Apollo DN10000.
3) The layout-to-circuit extraction makes it easy to generate circuits and to study device behaviour for different layouts.
4) Because a circuit simulator is used, the generated 3D model can be simulated together with external components.

References

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