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Optimization of DMOS Transistors for Smart Power Technologies by Simulation and Response Surface Methods

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Abstract

DMOS transistors for smart power technologies were investigated by extensive use of process and device simulation. For the task of simultaneously optimizing a multitude of parameters, experimental designs and response surface methods were used.

1. Introduction

The necessity to reduce development time and costs in the semiconductor industry enforces an increase in simulation efforts. CMOS technologies constitute the main driving force for the development and implementation of advanced physical models. Beside these advanced technologies, smart power technologies have gained much interest in recent years [1,2,3]. Although from the point of view of physical modeling not as demanding as e.g. far submicron CMOS, these technologies pose severe difficulties due to their complexities, the variety of devices and the combination of high voltage/power with logic and analog circuit capabilities.

The DMOS transistor is of central importance in smart power technologies. Fig. 1 shows a DMOS cell together with the periphery of the cell field. Targets for optimization include threshold voltage, saturation current, on-resistance, and breakdown voltage. These targets are influenced by process parameters, for instance epi thickness and concentration, body implant and body and source diffusion, and geometrical parameters such as cell dimension and poly field plate length on field oxide. The task of simultaneously optimizing a multitude of parameters leads to departing from the traditional "one-factor-at-a-time" method and to using statistical methods instead [4].

Extensive simulation was used to optimize such a device. Simulations were carried out with SUPREM-3 [5], TSUPREM-4 [6], and MEDICI [7]. Parameters were calibrated using experimental data. Fig. 2 compares simulated and measured values of threshold voltage. A systematic difference between both data sets can be seen, which may be

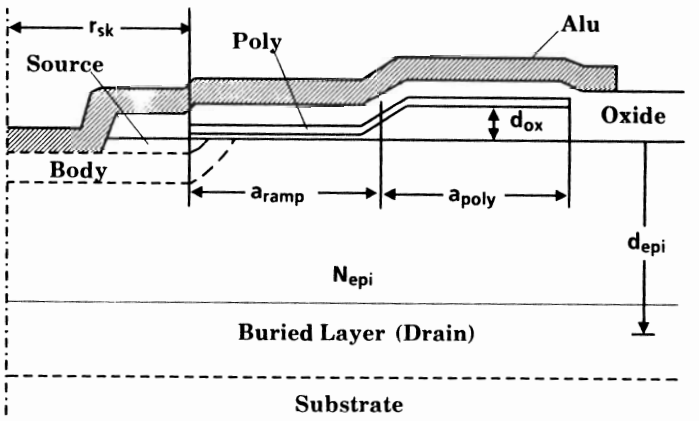

Figure 1: DMOS cross section. Half of the inner cell and periphery are shown. Process and geometrical parameters as used in the optimization of breakdown voltage are indicated (see text).

explained by oxide charge and other effects that were not taken into account in the simulation.

The factors with the major influence vary according to the targets chosen. Therefore, different experimental designs were used for intrinsic device performance data (inner DMOS cell) and breakdown optimization (peripheral structure).

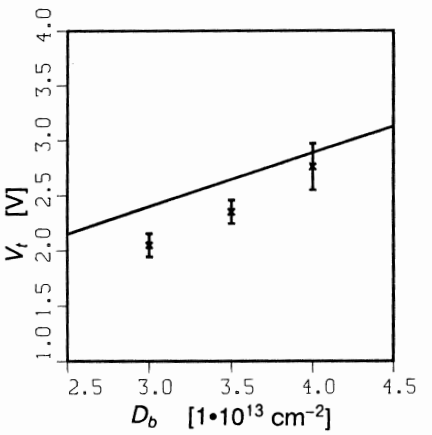

Figure 2: DMOS threshold voltage as a function of body implant dose. Comparison of simulated and experimental data.

Four factors were taken into account for threshold voltage: body implant dose (D_b) and energy (E_b), body (t_b) and source (t_e) diffusion time. Fig. 3 shows contour lines for constant threshold voltage as a function of body implant dose and diffusion time. The other factors (E_b, t_e) are held constant.

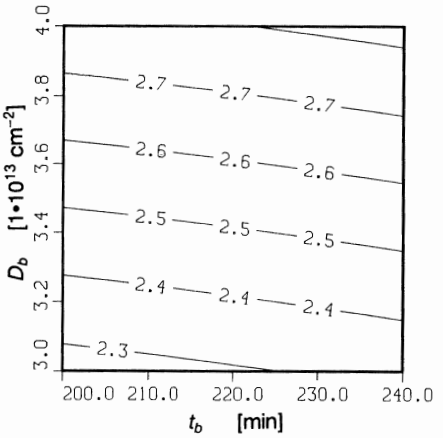

Figure 3: DMOS threshold voltage as a function of body implant dose and body diffusion time. Contour lines correspond to constant threshold voltage. Body implant energy and source diffusion time are kept constant.

The breakdown voltage is not only influenced by epi thickness (d_{epi}) and concentration (N_{epi}), but also by geometrical parameters. The gate polysilicon acts as a field plate to increase the breakdown voltage source/body to drain. A Box-Behnken design with the six factors as defined in Fig. 1 was used for the optimization. Fig. 4 shows contour lines for breakdown voltage as a function of d_{epi} and N_{epi}. For an assumed 10 percent variation of the process parameters the fitted polynomials obtained with the response surface method immediately give information on the corresponding variation of the target values, which is indicated in Fig. 4 by a box drawn around the central point.

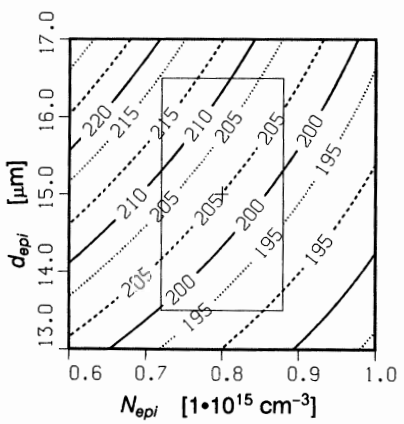

Figure 4: DMOS breakdown voltage. Contour lines of constant breakdown voltage as a function of epi thickness and concentration. Other parameters are held constant. Different line types correspond to different sets of parameters.

Fig. 5 gives an example of the influence of the geometrical parameters on the breakdown voltage. Contour lines as a function of cell contact dimension r_{sk} and distance

of the gate edge to field oxide a_{ramp} are shown. In this case, too, the contour lines correspond to a specific set of values for the other parameters.

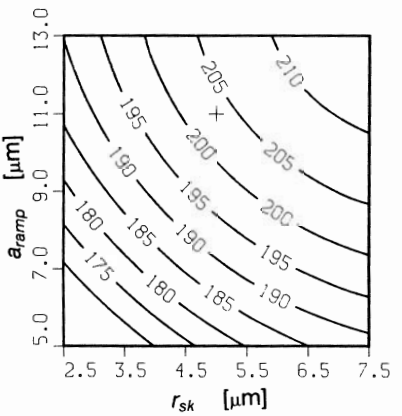

Figure 5: DMOS breakdown voltage. Contour lines of constant breakdown voltage as a function of cell contact length and distance of gate polysilicon edge to field oxide. Other parameters are held constant.

In conclusion we have used process and device simulation to optimize a DMOS transistor for a smart power technology. Classical simulation models are sufficient for this purpose, but the structures, nevertheless, constitute a challenge due to their complexities. Response surface methods were applied to efficiently treat several parameters simultaneously and thereby reduce computing resources.

References

[1] B. J. Baliga, IEEE Trans. Electron Devices, ED-33,1936(1986)

[2] A. Andreini, C. Contiero, and P. Galbiati, IEEE Trans. Electron Devices, ED-33,2025(1986)

[3] A. Preußger et. al., Proc. ISPSD 1991, p.195

[4] G. E. P. Box and N.R. Draper, *Empirical Model-Building and Response Surfaces*, John Wiley & Sons, New York, 1987

[5] TMA SUPREM-3 User's Manual, Technology Modeling Associates, 1990

[6] TMA TSUPREM-4 User's Manual, Technology Modeling Associates, 1991

[7] TMA MEDICI User's Manual, Technology Modeling Associates, 1992