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Numerical Simulation of MOSFETs Gate Capacitances for the Evaluation of Hot-Carrier Generated Interface States and Trapped Carriers

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Abstract

The two dimensional device simulation program MINIMOS is used to calculate gate-to-drain capacitance in the presence of spatially localised interface states and trapped charge. The program has been modified to allow for the introduction of donor and acceptor interface states in different parts of the band gap and with arbitrary spatial distribution along the channel. Numerical simulation and measurement results for gate-to-drain capacitance before and after stress are presented and compared. It is concluded that numerical study of the influence of each parameter on the gate capacitances as well as changes in I-V characteristics would provide a better understanding of the charges induced by hot carriers in a device.

1. Introduction

Hot-carrier generated interface states and trapped charges are the main causes of the degradation of MOSFET's under electrical stressing. Much work has been reported in the literature on the evaluation of these charges via the I-V characterisation of the device[1-3]. The information obtainable from these measurements is generally considered as incomplete, for example it is still unclear if the degradation is due to charge in the interface states or to charge of carriers trapped within the gate oxide. In this paper we present the numerical simulation study of the effects of interface states and trapped charges on the small signal gate-to-drain capacitance. This will demonstrate how the comparison of numerically simulated gate capacitances with the measured gate capacitances would enhance the understanding of observed device degradation due to hot carriers. In particular it will be shown that by comparing the simulated and measured gate capacitance one can obtain an indication of the spatial distribution of interface states and trapped carriers along the channel as well as the distribution in the energy band gap for interface states.

2. Experimental Results

The gate-to-drain capacitance C_{gd} of n-channel MOSFET with L=1.7μm and W=50μm was measured using a Hewlett-Packard 4284A LCR meter as a function of the dc bias before and after electrical stressing of the drain[4]. Fig. 1 (a) shows the measured C_{gd} before and after stress. Increase in C_{gd} after stress in the weak inversion regime is attributed to the presence of positive charge in the oxide near the drain. Conversely the decrease in C_{gd} in the strong inversion is due to negative charge in the oxide at the same location. Positive charge decreases the local threshold voltage V_T and leads to lower channel resistance near the drian. Whereas negative charge increases the local V_T and leads to higher channel resistance.

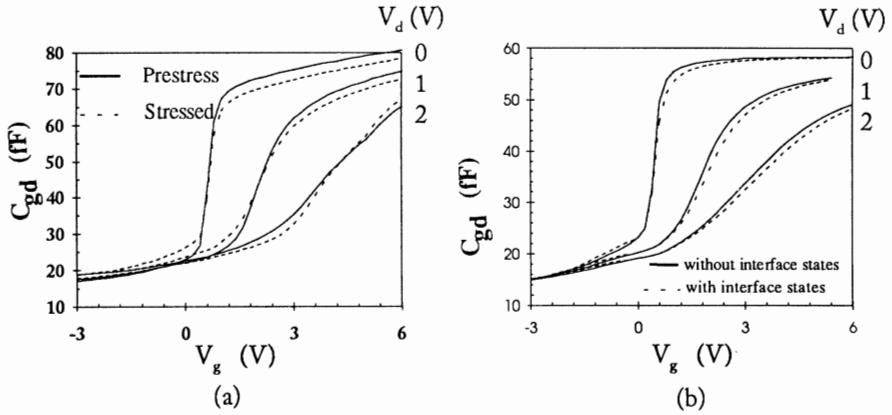

Fig. 1 (a) Measured C_{gd} versus V_g for n-MOSFET, stress condition: V_d=8 V, V_g=2 V, stress time=1800s. (b) Simulated C_{gd} versus V_g with and without interface states, see Fig. 3 for interface state distribution.

Fig. 2 (a), (b) and (c) show the variation of ac channel potential in response to an ac signal, V_{sig} applied to the drain, for (a) no charge, (b) positive charge and (c) negative charege near the drain. In each case C_{gd} is given by the shaded area of the graph:

$$C_{gd} = \frac{W \cdot C_{ox}}{V_{sig}} \cdot \int_{x=0}^{x=L} V_{ac}(x)\, dx$$

where C_{ox} is the gate oxide capacitance per unit area, W is the width of transistor, L is the length of transistor and x is the distance along the channel from the source to drain.

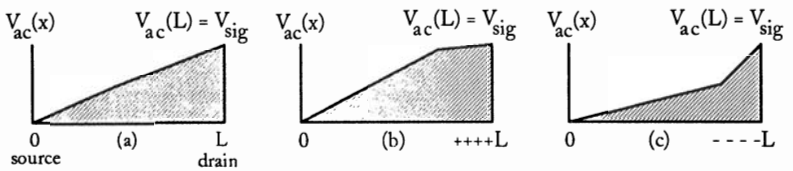

Fig. 2 AC channel potential profile showing the effect of charge in the oxide near drain: (a) with no charge, (b) with positive charge, (c) with negative charge.

As the sign of the charge is observed to vary with biasing condition a possible cause for this observation is the existence of both donor type and acceptor type interface states generated after electrical stressing located in different energy levels in the band gap. Due to the complexity of the problem the only way to examine this hypothesis is the use of numerical simulation.

3. Numerical Simulation Results

The two dimensional device simulator program MINIMOS is used to calculate C_{gd} in the presence of spatially localised interface states. The program has been modified to allow for the introduction of donor and acceptor interface states in different parts of the band gap as well as in different part of the channel.

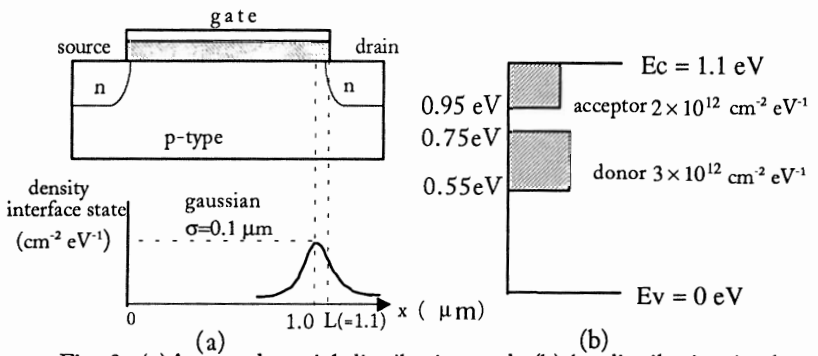

Fig. 3 (a)Assumed spatial distribution and (b)the distribution in the energy band gap of the interface states for the simulated device.

Fig. 1 (b) shows simulated C_{gd} versus gate voltage for different drain voltages with and without interface states. The assumed spatial distribution and the distribution in the energy band gap of the interface states is shown in Fig. 3. The simulation results confirm that the assumed interface state model does give rise to increased C_{gd} in low gate voltages and decreased C_{gd} in higher gate voltages (inversion).

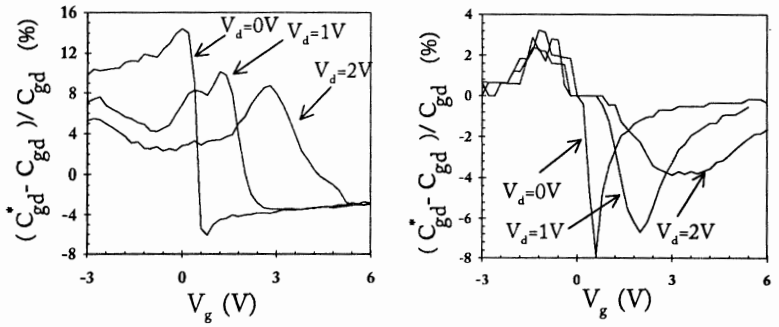

Fig. 4 (a) Percentage change in measured C_{gd} after stress versus V_g.
(b) Percentage change in simulated C_{gd} due to interface states versus V_g.

The fractional change in C_{gd} for measurement and simulation data is shown in Fig. 4. The agreement between measurement and simulation is not very good. In particular the positive peaks for the measurement case move to higher gate voltages as V_d is increased. This is not true for the simulated capacitances. This is due to the fact that the donor states are always occupied in the weak inversion regime regardless of the value of the drain voltage so their effect is not observable in the change in the C_{gd}.

It was found that an increase in C_{gd} in the weak inversion regimes after electrical stressing necessitate the existence of positive fixed charges or trapped holes near the drain junction. These positive fixed charges would then be compensated by the existence of the charges due to acceptor states in strong inversion. It was found that the interface states and fixed charge model shown in Fig. 5 (a) would produce best approximation to the observed change in C_{gd} before and after stress. The fractional change in C_{gd} for measurement and simulation data for the above model is shown in Fig. 5 (b).

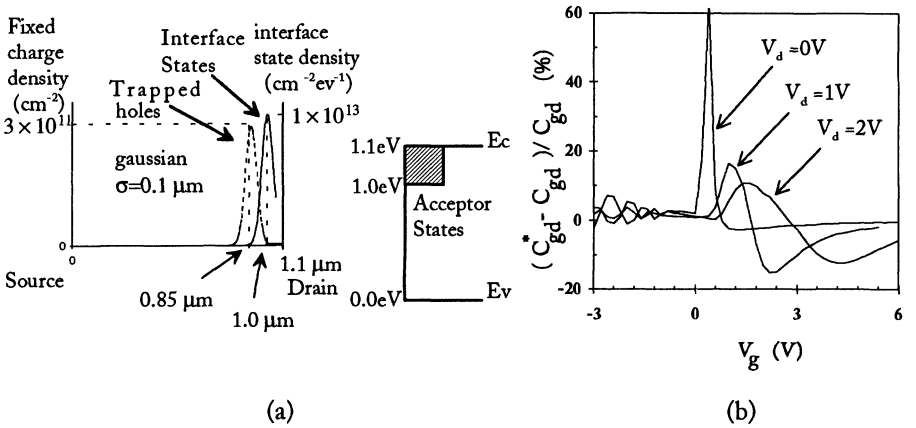

Fig. 5 (a) Assumed spatial distribution and the distribution in the energy band gap of the interface states for the simulated device. (b) Percentage change in simulated C_{gd} due to trapped holes and acceptor states versus V_g.

4. Conclusion

It is concluded that comparison of the numerically simulated gate capacitances with the experimental gate capacitances before and after stress can give us an indication of the nature, magnitude and spatial location of hot-carrier generated interface states and/or trapped carriers for different stress conditions. It can also provide information in regard to the distribution of the interface states in the energy band gap of silicon.

References

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