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Improved Technology Understanding through Using Process Simulation and Measurements

T. Feudel, W. Fichtner, N. Strecker, R. Zingg, G. Dallmann[†], and E. Döring[‡]

Integrated Systems Laboratory, ETH-Zürich
Gloriastraße 35, CH-8092 Zürich, SWITZERLAND
[†]Institut Fresenius, Angewandte Festkörperelektronik GmbH
Königsbrücker Landstraße 159, D-01109 Dresden, GERMANY
[‡]EM Microelectronic Marin SA
Rue des Sors 3, CH-2074 Marin, SWITZERLAND

Abstract

This paper will provide an example for improved technology understanding through a combination of simulation and measurements. Sample mispreparations and design errors could be detected very fast with process simulation, an extremly helpful tool to correlate physical and electrical measurements.

1. Introduction

In the past few years, process and device simulation has become indispensable for the development of semiconductor technologies. In contrast to device simulation, however, process simulators sometimes lack in accuracy and robustness. The reason is that many effects cannot be measured directly, especially in multi-dimensional (2D and 3D) situations. In order to be useful a modern process simulation environment must fulfill at least two criteria: (1) the physical models have to be accurate because of the shrinking device dimensions, and (2) to realistically describe influences between neighboring structures, large areas have to be handled. In this contribution, we present our approach in successfully applying a simulation environment together with sophisticated characterization techniques to the development of a complex VLSI BiCMOS process.

2. Device Technology

In a joint effort between the Integrated Systems Laboratory and EM, a modular BiCMOS technology is being developed, suitable for both low voltage (1.5 V) and high voltage (up to 120 V) analog-digital applications. Apart from conventional (5 V) n- and p-channel MOS devices, a variety of different bipolar and FET devices have been designed (e.g. vertical npn, lateral and vertical pnp transistors, JFET, EMOS, DMOS, diodes, resistors).

3. Simulation and Experiments

Compared with a conventional VLSI CMOS process, this BiCMOS technology is considerably more complex. As examples, we might mention the formation of dual (n^+/p^+) buried layers, the epitaxial substrate, the base/emitter optimization for npn and pnp, and, last but not least, the highly intricate isolation schemes. For a first round of experiments, a complete set of design rules for the active device regions was "extracted" from a large number of process and device simulations. The fabrications resulted in good MOS devices and in poor, but working bipolar transistors. In the extreme cases of low n-well and low base implants, electrical measurements on npn transistors gave an Early Voltage of 2 V, a current gain of 1000, a collector-emitter breakdown voltage of 4.5 V and a relatively high leakage current (nA) from base to substrate.

Therefore a second round of simulations was necessary. For this, we have used a system which automatically performs 1D and 2D simulations based on design information (CIF files, Fig. 2) and the process description [1]. Our in-house simulators TESIM (1D) and DIOS (2D) provide a consistent model base, which has been verified for this process by a series of SIMS, SEM and EBIC measurements. Figure 1 shows a comparison of SIMS and TESIM results for the p-base with and without the influence of the n^+-emitter. In this case, no emitter dip effect could be found.

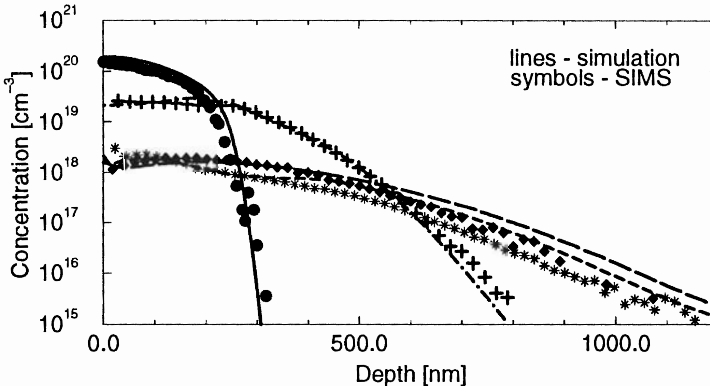

Figure 1: Cut through emitter (As: filled circles and solid lines, P: crosses and dash dotted, B: stars and short dashed) and base region (B: diamonds and long dashed)

Using the advanced automatic grid adaption strategies of DIOS and a modified pragmatic approach for local oxidation [2] of arbitrary shaped structures, rather complex "complete" BiCMOS devices including isolation areas could be simulated in a single run. Fig. 2 shows the cross-sectional view of an n-p-n transistor (65k grid points, 25 CPU-h on a SUN-Sparcstation 10).

Both the simulation and the EBIC images show the reason for the high leakage currents in the too low doped n-well (upper right corner of Fig. 2 and 4). Also shown are n^+-regions on the lateral borders of the p-base regions because of a too small polysilicon width. The reason for the low breakdown voltage has been found in the strong influence of the n^+-buried layer on the active areas. In this case, the EBIC image showed a junction depth for the buried layer of 12 μm and a plateau in the linescan profile at 7.5 μm detecting an internal electric field maxima (Fig. 3). This

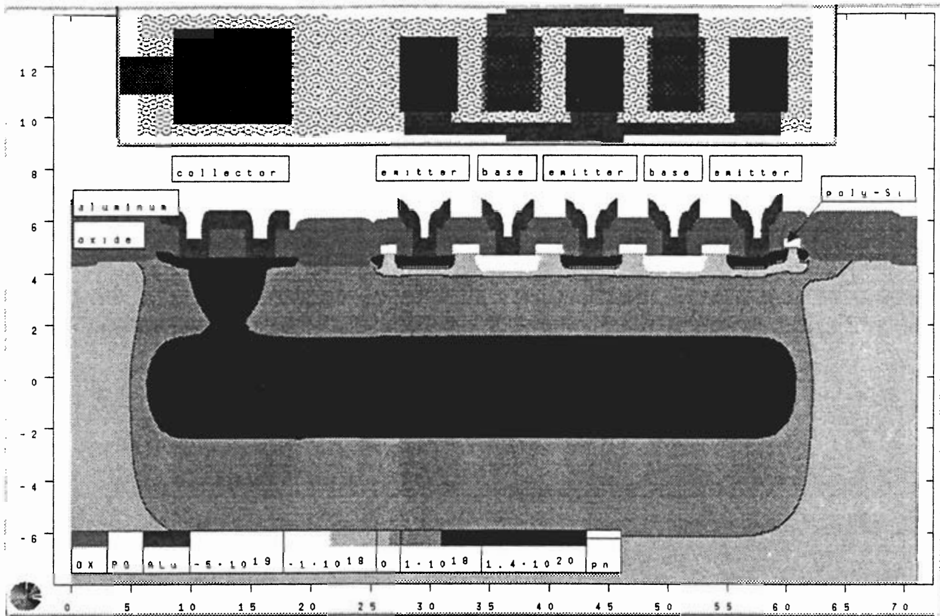

Figure 2: Layout and cross section of a simulated n-p-n transistor

was in bad agreement with first simulation results. The reason was found through the SIMS profiles showing an additional phosphorus implant below the arsenic buried layer. This implant could be traced to an error in the process flow.

4. Conclusions

The simulation system has been shown to be robust enough for automatic simulation of large BiCMOS structures. It was necessary to improve the grid adaption strategies and to refine the 2D oxidation models to handle complex device structures. A comparison with experimental data showed the bottlenecks of the used technology. Especially EBIC was found to be a valuable technique for the characterization of the 2D shape of pn-junctions.

Acknowledgement

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References

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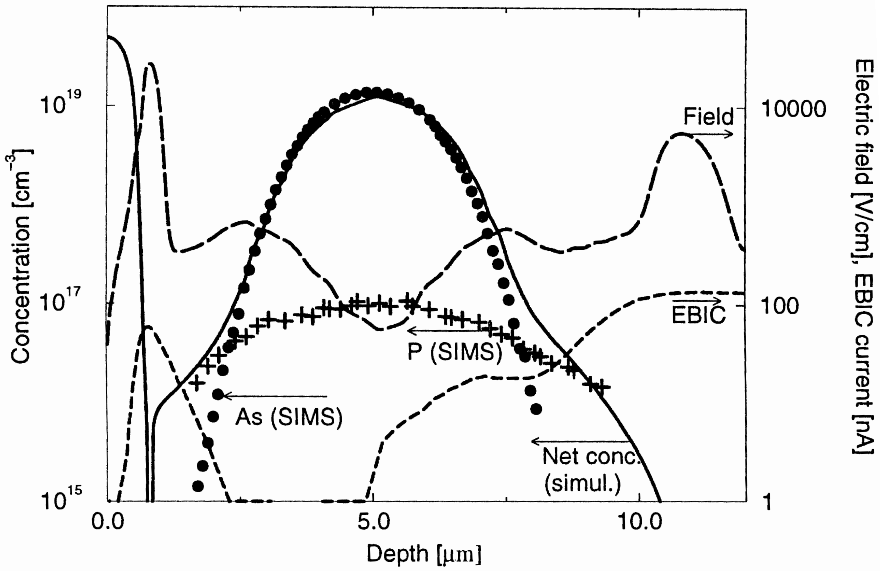

Figure 3: Measured (SIMS, EBIC) and simulated (net doping, electric field) profiles in the base contact region

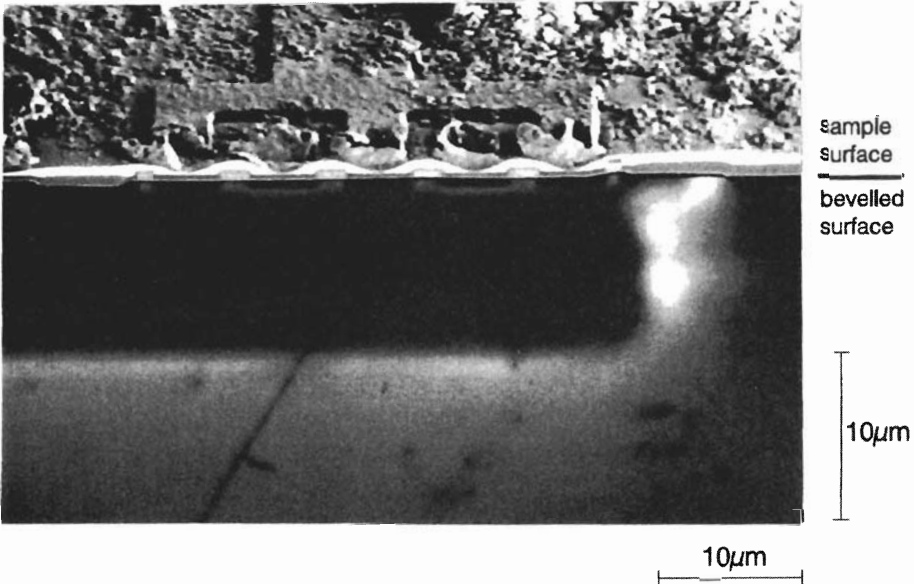

Figure 4: SEM and EBIC images of the bevelled n-p-n transistor (beam voltage 3 kV)