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Evaluation of Effective Device Parameters by Comparison of Measured and Simulated C-V Characteristics for Conventional and Pseudomorphic HEMTs

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Abstract

Measurements of the gate C-V characteristics of several conventional and pseudomorphic high electron mobility transistors (HEMT) on wafer and the comparison with simulations are presented. In order to study the influence of important technological parameters on the capacitance, the Schrödinger and Poisson equations were solved self-consistently in the structure, using the thickness of the doped layer d_A, the doping density N_D and the built-in voltage V_b as fit parameters. Measurement and simulation were found to be in good agreement and the fit parameters can be shown to be the effective device parameters. We demonstrate how to apply this technique for monitoring the spatial variation of d_A, N_D and V_b over the wafer, a result of particular importance for the development of the manufacturing process and for calibrating the design of the device.

1. Introduction

It is well known that the shape of the gate capacitance C_g versus gate voltage V_g relationship of heterojunction devices is strongly influenced by the properties of the quasi two-dimensional electron gas (Q2DEG) which forms the active region of the device [1, 2]. Another important contribution to the capacitance is given by the change of the ionized donor concentration in the doped layer, as well as by the onset of a so-called parasitic channel in the wide bandgap material. The one-dimensional self-consistent Schrödinger-Poisson solver (SPS) computes the charge distribution and the layer capacitances for arbitrary conventional or pseudomorphic heterojunction structures. Only physical parameters like the effective electron masses, the dielectric constants of the different materials and the conduction band-edge discontinuities forming the heterojunction were used as input parameters in addition to the thickness of the different layers and the doping densities. SPS is also able to take into account the three conduction band valleys (Γ, X, L), the local exchange-correlation potential and deep donor levels according to the model of Schubert and Ploog [3]. The physical parameters used for the modelling are described in the literature (Table 1, [1, 4, 5, 6]). For the heterojunction band-edge discontinuity we used a $\Delta E_c = 0.65\ \Delta E_g$ rule [6]. The solution of the Schrödinger equation follows a description of P.C. Chow [7].

Measurements were performed on wafer on conventional $Al_{0.23}Ga_{0.77}As/GaAs$ and pseudomorphic $Al_{0.23}Ga_{0.77}As/In_{0.2}Ga_{0.8}As/GaAs$ HEMTs using an HP 4275 A impedance analyzer. The source and the drain contacts were set to the same potential for the measurements and the measurement frequency was 1MHz.

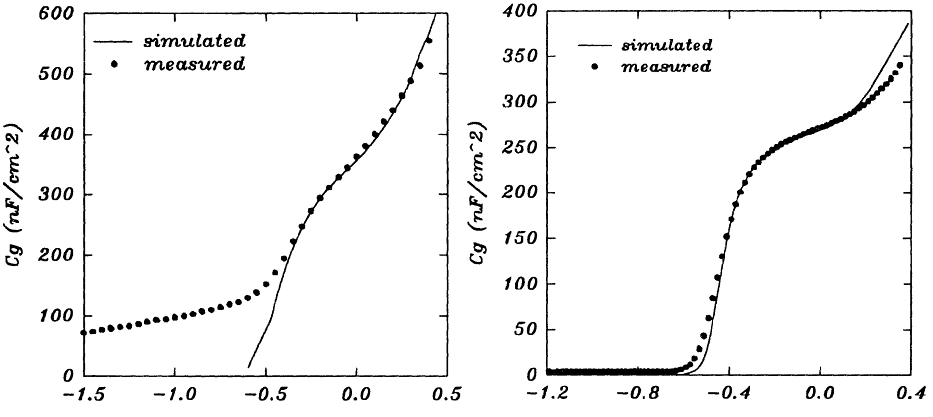
The nominal thickness for the supply layer was designed to d_A = 40 nm (Table 1). This thickness d_A is sometimes affected by etching process steps while forming the gate on top of the supply layer. A reduction of the effective d_A influences all electric properties of the device, including the gate capacitance.

Layer	x, y	d (nm)	$N_{D,A}$ (cm^{-3})	E_g (eV)	m^*/m_0	$\varepsilon/\varepsilon_0$
$Al_xGa_{1-x}As$-supply	0.23	40	1.5E18 (D)	1.711	0.084	12.4
$Al_xGa_{1-x}As$-spacer	0.23	2	0	1.711	0.084	12.4
$In_yGa_{1-y}As$-channel	0.2	12	0	1.140	0.058	13.2
GaAs-buffer	—	>1000	2.4E14 (A)	1.424	0.067	13.1

Table 1: Nominal process parameters for a pseudomorphic HEMT and physical parameters used for the simulations. Same for conventional HEMTs, but without $In_yGa_{1-y}As$-channel layer.

2. Results

The gate C-V characteristics measured on sub-μm gate-length transistors show significant contributions of pad and fringe capacitances (Fig. 1a). They agree very well



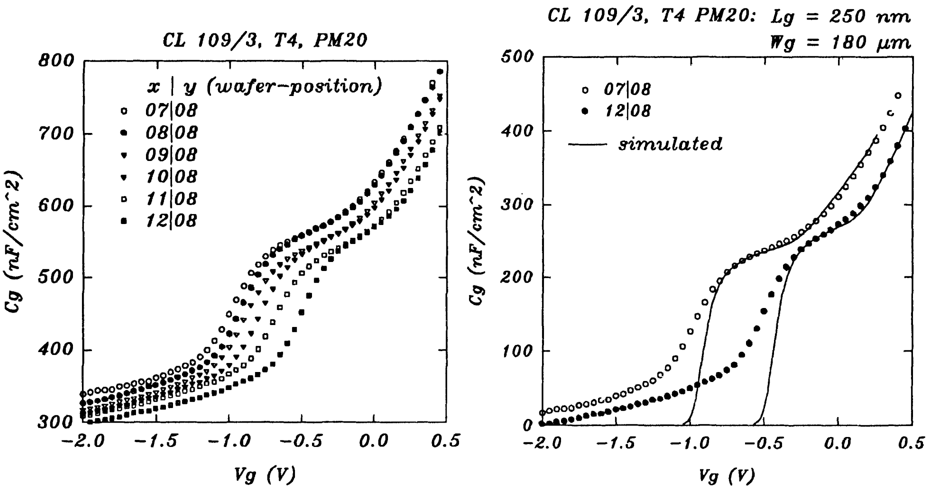
a) conventional HEMT with a sub-μm gate-length structure

b) pseudomorphic HEMT with a 100 μm gate-length structure ("fat FET").

Figure 1: Examples for the comparison between simulated and measured gate C-V characteristics of conventional and pseudomorphic HEMTs.

with the SPS simulation above the threshold voltage. Pad capacitances were assumed to be constant over the observed voltage range and could be subtracted from the measurement signal. The remaining contribution to the capacitances at negative voltages was assumed to be mainly due to fringe capacitances. If measurements are performed on so-called fat FETs (gate-length 100 μm) the pad and fringe capacitances do not contribute significantly to the data (Fig. 1b).

Moreover, the C-V characteristics measured on the fat FETs agree very well with the SPS simulation over the whole voltage range. If measurements were performed on sub-μm gate-length transistors (L_g = 250 nm, W_g = 180 μm) across a wafer, a systematic displacement between the curves measured in the outer and in the inner regions of the wafer was found (Fig. 2a). The origin of this displacement was assumed to be an irregularity in one of the manufacturing process steps. By comparison of the measured data with SPS simulations (Fig. 2b) we could show that the displacement of the measured C-V characteristics resulted from a systematic change of the effective thickness d_A of the doped AlGaAs layer in the pseudomorphic HEMTs (Table 2). The doping concentration N_D as well as the built-in voltage V_b were found to be fairly constant over the wafer.



a) Measured capacitances from the outer (right curve) to the inner (left curve) region of the wafer

b) Comparison between selected curves and simulations

Figure 2: Measurement and simulation of the gate capacitances of pseudomorphic HEMTs.

Device #	d_A (nm)	N_D (cm^{-3})	V_b (V)
07|08	37	1.5E18	1.0
12|08	32	1.5E18	1.1

Table 2: Parameters evaluated from the simulations shown in Fig. 2b

This result could be corroborated e.g. by SEM photographs which showed that the thickness of the doped layer d_A was indeed diminished by several etching steps. In addition, it explains systematic shifts in other HEMT electrical properties (e.g. the transfer characteristic) we found when measurements were performed across the wafer. Consequently, the evaluated fit parameters were taken to be the effective device parameters. Furthermore, the comparison of measured and simulated C-V characteristics and the resultant effective device parameters led to an improvement of the manufacturing process.

3. Conclusion

We have developed a one-dimensional self-consistent Schrödinger-Poisson solver (SPS) which is capable of simulating the charge control behaviour and the associated capacitances for arbitrary heterojunction structures. The gate-to-source capacitances of several conventional and pseudomorphic HEMTs were measured and compared with C-V characteristics simulated by SPS. A very good agreement between measurement and simulation of the C-V characteristics was found for so-called fat FET structures over the whole voltage range, as well as for sub-μm gate-length transistors for voltages higher than the threshold voltage. When measurements were performed across a wafer a systematic displacement of the C-V characteristics was found. It could be shown by comparison of measured data with SPS simulations that this displacement was mainly due to a variation of the effective thickness of the doped layer d_A over the wafer. The method described above can easily be used for the evaluation of effective device parameters. This is a result of particular importance for the design of the device and the development of the manufacturing process.

Acknowledgements

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