

The Influence of Technological Parameters on Ultra-Short Gate Si-NMOS Transistor Performances

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Abstract

We have studied the effect of technological parameters on the performances of an ultra-short Si-NMOS transistor, at room temperature, using 2D Monte Carlo simulation. Results obtained for a device with source-drain extensions are compared with experiments. Doping profiles of Gaussian form are assumed. The main physical phenomena involved in the device behaviour are described. Additionally, electrical characteristics are analysed (transconductance, threshold voltage, cut-off frequency). Transconductance of 600mS/mm and intrinsic cut-off frequency close to 300Ghz are obtained for a NMOS structure with optimized source drain extensions and 0.07 μ m gate length.

1. Introduction

We used a 2D Monte Carlo method [1, 2] to study the influence of technological parameters on the performances of ultra-short gate NMOS transistor including source-drain extension (SDE) [3] in order to define an optimized structure. The structure, sketched in figure 1, has a gate oxide thickness of 45Å, a junction depth of 0.1 μ m. The SDE doping profile is Gaussian with maximum concentration at a projected range R_p , a parallel standard deviation ΔR_p and a transverse standard deviation ΔR_t close to 800Å and 400Å respectively. The channel doping profile is also Gaussian. The doping level is 10^{19}cm^{-3} for the heavily doped region. A uniform substrate doping concentration of 10^{16}cm^{-3} is used. The Si/SiO₂ interface presents uniform surface states Q_{ss} close to $3 \cdot 10^{10}\text{cm}^{-2}$ and fixed oxide charges Q_{ox} [4]. The substrate and source are assumed to be grounded. We will focus on the physical information and the performances of device extracted from the simulation and their comparison with experimental data at room temperature [3].

2. Influence of Source-Drain Extensions

In this section, we assume channel profile parameters: $DI=2 \cdot 10^{12}\text{cm}^{-2}$; $R_p=100\text{Å}$; and $Q_{ox}=3 \cdot 10^{10}\text{cm}^{-2}$.

2.1. Influence of Source-Drain Length L_z

We have presented in figure 2, the dependence of the drain current on gate voltage, for two different values of the source drain extension length L_z (0.12 μ m and 0.07 μ m), with SDE doping profile parameters: $DI=10^{14}\text{cm}^{-2}$, and $R_p=100\text{Å}$. It should be noted that the gate charge control decreases if the extended zone length increases. As the length of the SDE increases, it introduces series resistance to source and drain, raising the electric field. This increased field is undesirable because it creates energetic carriers that degrade the velocity overshoot resulting in a limitation of the maximum voltage that can be used. Through a set of simulations, we found that the optimal value of the SDE length is close to 0.07 μ m.

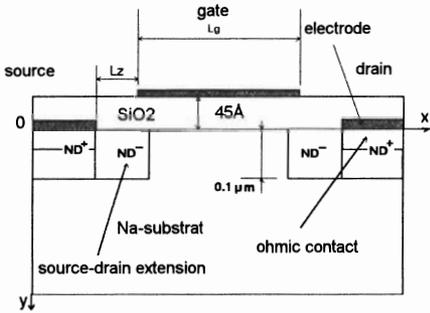


Fig 1 Schematic cross section showing simulated device structure with ultra-short gate.

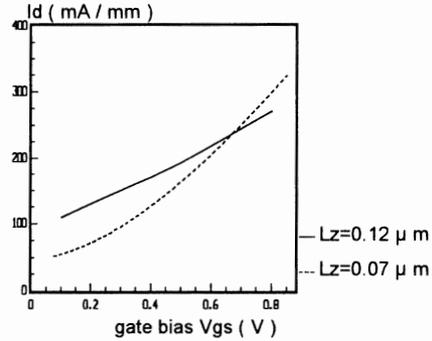


Fig.2 Transfer characteristics for two values of source drain extension length: 0.12μm and 0.07μm (Lg=0.1μm; Vds=1V).

2.2. Source-Drain Extensions Doping Profile

Now, we assume Lz parameter is 0.07μm. Figure 3 shows the evolution of the transconductance as a function of the applied gate voltage Vgs, for two implantation doses (10¹⁴cm⁻² and 5*10¹³cm⁻²). Projected range Rp of the SDE is 100Å. We observe a decrease of the transconductance with reducing doping level. This behaviour is caused by mobile charges deficiency in SDE zones and thus in the transistor channel. Figure 4 shows transconductance evolution with gate voltage for two values of the projected range: Rp=100Å and Rp=1000Å. The implantation dose of the SDE is 10¹⁴cm⁻². We observe that the conductance decreases when the distance between the maximum doping and the interface increases. This reduction is attributed to the spreading of carrier distribution into the semiconductor as the projected range increase.

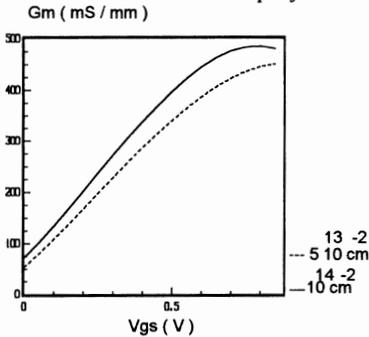


Fig.3: Intrinsic transconductance versus gate bias for two values of implantation ion doses in SDE: 10¹⁴cm⁻² and 5*10¹³cm⁻²(Lg=0.1μm Vds=1V).

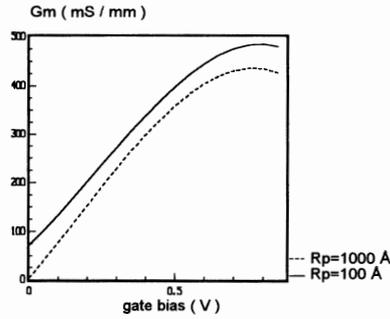


Fig.4: Intrinsic transconductance versus gate bias with two values of projected range: 100Å and 1000Å (Lg=0.1μm; ΔRp=800Å; ΔRt=400Å and Vds=1V)

In the following study, the parameters of SDE are: DI=10¹⁴cm⁻², Rp=100Å, Lz=0.07μm.

3. Threshold Shift

For n-channel MOSFET structure with positively biased gate a negative space charge appears in the semiconductor beneath the oxide. If the electron density at the surface is

equal to holes density, the potential applied to the gate is called reversal threshold voltage V_T . This parameter is very important in MOSFET's digital applications. We assume $Q_{ox}=3 \cdot 10^{10} \text{cm}^{-2}$ and study the threshold shift. Figure 5 shows the evolution of threshold voltage as a function of the channel implantation dose DI with $R_p=100\text{\AA}$. The tension V_T is proportional to DI . This behaviour is attributed to the diffusion of the channel electrons into the semiconductor as the implantation dose DI increases. Figure 6 shows the evolution of tension V_T in relation to the projected range R_p of channel profile with a channel implantation dose of $2 \cdot 10^{12} \text{cm}^{-2}$. We observe that the threshold voltage is proportional to R_p because the channel carriers density is spread into the device when the projected range increases. Now, we assume channel doping parameters of $DI=2 \cdot 10^{12} \text{cm}^{-2}$; $R_p=100\text{\AA}$ and study the effect of the oxide charges on threshold voltage. Figure 7 displays the evolution of threshold voltage as a function of oxide charge assuming that $Q_{ss}=3 \cdot 10^{10} \text{cm}^{-2}$. We observe a linear decrease of V_T versus Q_{ox} . This is produced by positive charges which attract more and more electrons to the surface, resulting in an earlier conduction in the channel.

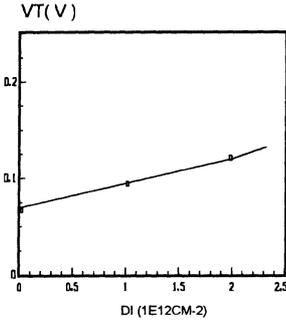


Fig.5 Threshold voltage versus channel implantation dose ($L_g=0.1\mu\text{m}$; $V_{ds}=1\text{V}$; $Q_{ox}=3 \cdot 10^{10} \text{cm}^{-2}$; channel doping parameters are $R_p=100\text{\AA}$ and $\Delta R_p=800\text{\AA}$).

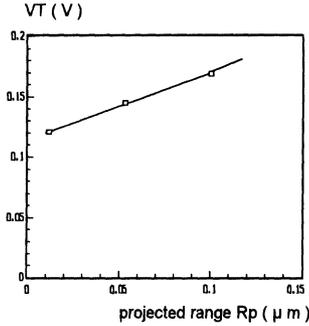


Fig.6 Threshold voltage versus projected range R_p of doping profile in the channel. ($L_g=0.1\mu\text{m}$; $V_{ds}=1\text{V}$; $Q_{ox}=3 \cdot 10^{10} \text{cm}^{-2}$; $DI=2 \cdot 10^{12} \text{cm}^{-2}$).

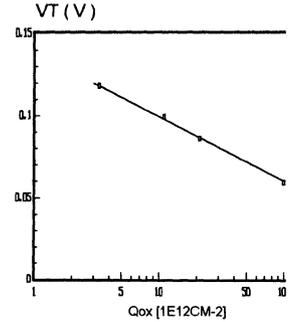


Fig.7 Threshold voltage versus oxide charges. ($L_g=0.1\mu\text{m}$; $V_{ds}=1\text{V}$).

4. Influence of the Gate Length

In this paragraph, we consider that the channel doping profile parameters are: $DI=2 \cdot 10^{12} \text{cm}^{-2}$, $R_p=100\text{\AA}$ and $Q_{ox}=3 \cdot 10^{10} \text{cm}^{-2}$.

Figure 8a shows the evolution of V_T in relation to the gate length. We notice that, when the gate length decreases, threshold tension decreases also because channel conduction is favoured by carrier diffusion between source and drain. In figure 8b is presented the evolution, with gate length, of the maximum transconductance obtained both theoretically (MC and Drift Diffusion (DD) simulation) and experimentally [1]. For gate length larger than $0.07\mu\text{m}$, the MC results are in a good agreement with experiments. The differences between MC and DD results increases with decreasing gate length. This is due to the non-stationary transport which is not accounted for in the DD model. In ultra-short gate length devices this is the dominant mechanism. For gate length shorter than $0.07\mu\text{m}$, electrons are not able to reach their maximal non-stationary velocity (figure 9). This results in a reduced gate control and G_m decreases with decreasing gate length. Thus the optimized gate length should be close to $0.07\mu\text{m}$ and transconductance of 600mS/mm could be achieved.

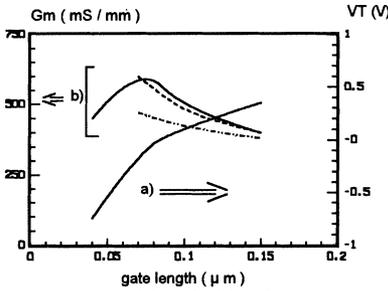


Fig. 8 a): Threshold voltage versus gate length ($DI=2*10^{12}cm^{-2}$; $Q_{ox}=3*10^{10}cm^{-2}$). b): Intrinsic maximum transconductance versus gate length ($V_{ds}=1V$). --- exp. Sai-H. -.- drift diffusion ___ monte carlo

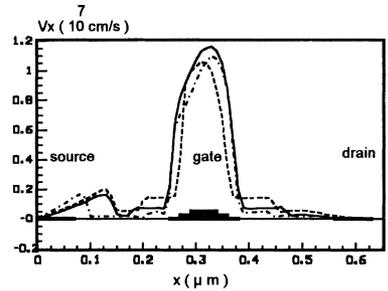


Fig. 9: Average velocity along the channel for three values of gate length: --- $L_g=0.04\mu m$; $L_g=0.07\mu m$; -.- $L_g=0.1\mu m$ ($V_{ds}=1V$; $V_{gs}=0.8V$). Average velocity defined by: $\langle v_x \rangle_y = \langle v_x \cdot n \rangle_y / \langle n \rangle_y$; where $\langle \bullet \rangle_y = \int \bullet dy$

The intrinsic cut-off frequency defined by:

$$F_c = \frac{G_m}{2\pi C_{gs}}$$

is presented in Figure 10. Reducing the gate length increase F_c , mainly due to a drastic reduction of gate capacitance C_{gs} . If we add parasitic capacitances to our calculation the F_c values ($\approx 300GHz$ for $L_g=0.07\mu m$) would be lower. This aspect yields an important reduction of cut-off frequency for experimental device [5].

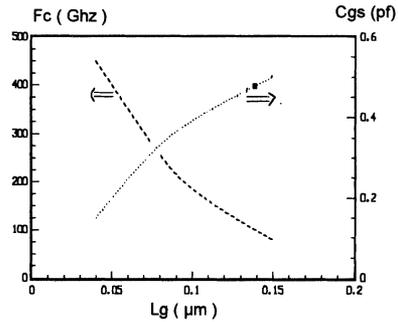


Fig.10: Intrinsic cut-off frequency and gate capacitance versus gate length ($V_{ds}=0.8V$).

5. Conclusion

We have used a Monte Carlo program to investigate the ultra-short gate Si-NMOS transistor performances. The results obtained by this model are in good agreement with experimental ones. Transconductance of 600 mS/mm and intrinsic F_c close to 300 Ghz could be obtained for a NMOS structure with optimized SDE region and $0.07\mu m$ gate length.

References

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