SIMULATION OF SEMICONDUCTOR DEVICES AND PROCESSES Vol. 5
Edited by S. Selberherr, H. Stippel, E. Strasser - September 1993

Hot Carrier Suppression for an Optimized 10V CMOS Process

A. Bauer, H. Noll, and H. Pimingstorfer†

Reasearch and Development, AMS Austria Mikro Systeme International AG
Schloß Premstätten, A-8141 Unterpremstätten, AUSTRIA
†Institute for Microelectronics, TU Vienna
Gußhausstraße 27-29, A-1040 Wien, AUSTRIA

Abstract

An advanced 2μm twin-well CMOS process for mixed analog/digital designs with operating voltages up to 10 Volts is presented. The process uses an optimized LDD-structure with high-energy n- implant for the n-channel transistors which drastically reduces the substrate current by a factor of approximately 50 compared to a standard 2μm/5V process technology. A number of relevant process parameters have been optimized to find the ideal balance between driving capability/speed and long-time reliability.

1. Introduction

The maximum supply voltage of most CMOS VLSI processes is limited to 5V or less. However, certain applications require higher operating voltages, e.g. telecommunication and data-conversion products with the need of an extended signal range or improved signal-to-noise ratio. Whilst a 5V process with 2μm channel length does not require advanced transistor design, a higher operating voltage can lead to similar problems as known in submicron process technology.

In order to achieve 10V supply voltage the substrate current and hot-carrier generation has to be reduced drastically. This will increase the bipolar breakdown voltage and ensures long-term reliability. In general, a smooth doping profile at the drain/channel junction gives a wider spread of the drain potential and reduces the electric field and therefore the hot-carrier degradation.

Further improvements can be obtained, if the main part of the drain current bypasses the high-field region, as both, hot-carrier degradation and substrate current generation are proportional to the carrier density [1]. The degradation is also a function of the distance of the hot-carrier generation center from the surface and the gate edge, so that a low substrate current value does not necessarily imply a long lifetime [2]. Therefore, besides the reduction of substrate current, it is absolutely essential, to develop a hot-carrier resistant structure as reported in [3, 4].

2. Process Development

The original 2µm/5V process uses a DDD-structure (doubly doped drain) for the n-channel transistors. At higher drain voltage, the substrate current increases rapidly and causes bipolar breakdown at about 8.5V. As a simple adjustment of the DDD-implant parameters did not provide any improvement, an LDD structure was introduced.

By using the PROMIS [5] and MINIMOS [6] simulation tools and statistical design of experiments a sensitivity analysis of the substrate current was carried out (Fig. 1, 2, 3). Based on this analysis and subsequent experiments a high-energy / low-dose LDD-implant (170keV, 5E12 to 1E13/cm²) with 0.5µm wide spacer was chosen. For this process condition, an exceptionally low substrate current was measured. It was reduced by a factor of 50-100 (1-2nA/µm measured at 5V) compared to the standard process (100-150nA/µm) with snapback voltages of more than 14 Volts.

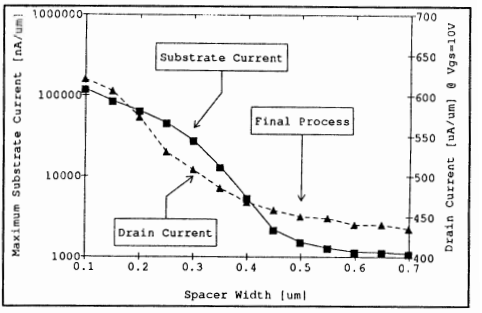

Fig. 1: Simulated substrate and drain current vs. spacer width (Vds=10V, LDD-implant parameters: 8E12/cm²/170keV).

The high implant energy is fairly uncommon in LDD technology but it seems to be a key parameter for this process. Unfortunately, without further attention, the implant may channel through the gate and generate low-threshold spots in the channel region resulting in increased leakage current or even shorted transistors. Measurements on dedicated test structures showed that this behavior occurs 10-50 times for 10^6µm of transistor width. Oxidizing the polysilicon (about 50nm) before doing the LDD-implant reduced the probability to 0.1-1 defects per 10^6 µm gate length - but this was still unacceptable.

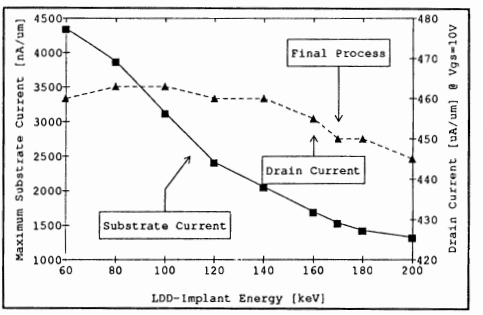

Fig. 2: Simulated substrate and drain current vs. LDD-implant energy (Vds=10V, implant dose=8E12/cm², spacer width=0.5µm).

The problem was avoided by using the remaining photoresist which is left on top of the polysilicon after gate-etch, as a self-aligned implant mask. As the n-channel LDD-implant also goes into the p-channel source/drain regions, a p-LDD implant (1E13/cm² dose) has been added for compensation.

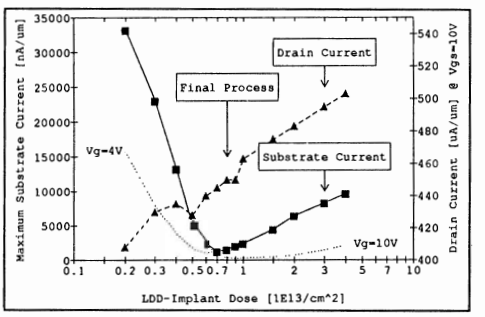

Fig. 3: Simulated substrate and drain current vs. LDD-implant dose. (Vds=10V, implant energy=170keV, spacer width=0.5µm).

Beside the p-LDD implant, process modifications for the p-channel transistors involve a shallow, high-dose (6E15/cm²,

55keV) BF_2 source/drain implant. The implant is driven by the full source/drain diffusion (1000°C, 50min) under the spacer to form a smooth doping profile at the drain junction which effectively suppresses PMOS hot-carrier generation.

The final process parameters were optimized for maximum driving capability at minimum 10 years extrapolated DC lifetime (10% gm degradation) under all bias conditions [7].

3. Process and Device Simulation

The effective suppression of substrate current is due to the fact that the drain current is not coincident with the location of the electric field maximum. The peak lateral field is located deep in the substrate (Fig. 4a) and remains nearly unchanged as the gate voltage is swept from average to high voltage.

At low gate voltage the drain current bends down after leaving the channel and bypasses the high-field region (Fig. 4b). As a result the carrier-generation rate is low and also sufficiently far away from the surface (Fig. 4c). As the gate voltage is increased the drain current increases but shifts towards the surface. Overall, the integral carrier-generation rate is reduced.

The balance of the reduction of the electric field and the increase of current-density depends on the LDD-implant dose. For a lower implant dose the substrate current curve bends up again at high gate voltages (Fig. 5). As at high gate voltages the center of hot-carriers also comes closer to the surface, it is obvious, that the device is more sensitive for this bias-condition. Actually, a bad lifetime has been measured for the $5E12/cm^2$ group at high gate voltages. This behaviour is reproduced by simulation quite well (Fig. 6).

It has been reported, that the upward-bending of the substrate-current curve is related to an electric-field peak on the source side resulting primarily from a low n- implant dose [8]. For our process, we did not observe a significant electric-field peak nor carrier-generation at the source. Instead, simulation shows that the carrier density becomes comparable to the n-doping concentration at high gate voltage. Therefore, the potential drop is shifted from the LDD region to the n-/n+ section which results in an increase of the electric field.

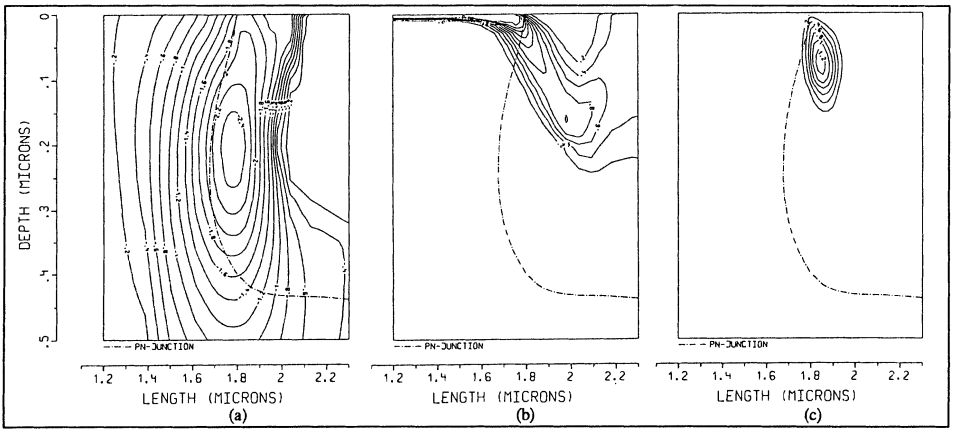

Fig. 4: Simulated electric field (a), electron current (b) and carrier generation (c) for LDD-implant parameters $8E12/cm^2$, 170keV (Vds=10V, Vgs=4V).

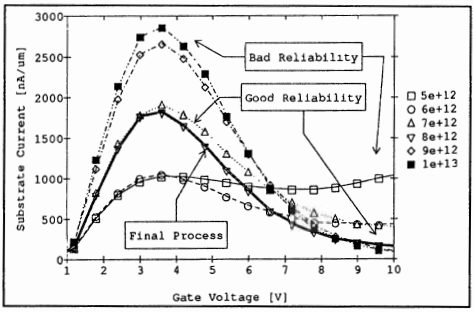

Fig. 5: Measured substrate current vs. gate voltage var. LDD-implant dose (Vds=10V).

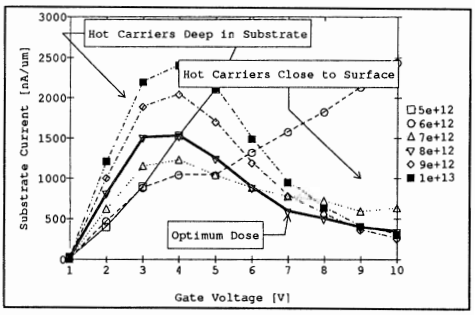

Fig. 6: Simulated substrate current vs. gate voltage var. LDD-implant dose (Vds=10V).

4. Conclusions

The development of a new 10V CMOS process has been presented. The LDD-structure itself and the integration in the standard process was optimized by means of process and device simulation and statistical design of experiments.

Except for the improved breakdown behavior and the reduced substrate current all electrical parameters are very close to the original 2µm/5V process. The process does not require any special design rules. Therefore, almost all standard-cell libraries can be used without any modification.

References

[1] M.-L. Chen, C.-W. Leung, W. T. Cochran, W. Jüngling, C. Dziuba and T. Yang, "Suppression of Hot-Carrier Effects in Submicrometer CMOS Technology", IEEE Trans. Electron Devices, vol. 35, no. 12, 1988, p. 2210.

[2] W. Hänsch, C. Mazure, A. Lill and M. Orlowski, "Hot Carrier Hardness Analysis of Submicrometer LDD Devices", IEEE Trans. Electron Devices, vol. 38, no. 3, 1991, p. 512.

[3] J. Hui and J. Moll, "Submicrometer Device Design for Hot-Electron Reliability and Performance", IEEE Electron Device Lett., vol. EDL-6, no. 7, 1985, p. 350.

[4] J. J. Sanchez, K. K. Hsueh and T. A. DeMassa, "Drain-Engineered Hot-Electron-Resistant Device Structures: A Review", IEEE Trans. Electron Devices, vol. 36, no. 6, 1989, p. 1125.

[5] G. Hobler, S. Halama, W. Wimmer, S. Selberherr and H. Pötzl, "RTA-Simulations with the 2D Process Simulator PROMIS", Proc. NUPAD III, 1990, p. 13.

[6] S. Selberherr, "Three Dimensional Device Modeling with MINIMOS 5", Proc. Int. Workshop on VLSI Process and Device Modeling, 1989, p. 40.

[7] A. Bauer, H. Noll, H. Pimingstorfer, "Optimizing Reliability of a 10V CMOS Process Using Process and Device Simulation", Proc. IASTED Modelling and Simulation, 1993.

[8] M. K. Orlowski, C. Werner and J. P. Klink, "Model for the Electric Field in LDD MOSFET's - Part I: Field Peaks on the Source Side", IEEE Trans. Electron Devices, vol. 36, no. 2, 1989, p. 375.