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Modeling of Breakdown in SOI MOSFETs

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Abstract

This paper describes how a modified version of the two-dimensional device simulator MINIMOS4 has been used to simulate the dependence of the breakdown voltage in an SOI transistor on key device parameters. The strong influence of the gain of the parasitic lateral bipolar transistor is discussed.

1. Introduction

Silicon-on-insulator (SOI) MOSFETs suffer from low operating voltages as a result of an enhanced breakdown due to the lateral bipolar transistor[1]. Breakdown occurs when the product of the bipolar current gain β and avalanche multiplication rate M-1 tends to unity. As the drain voltage is increased, accumulation of positive charge in the film causes the threshold voltage to reduce, progressively shifting the characteristics in the direction of lower gate voltage eventually leading to hysteresis[2]. By simulating these effects, it is possible to define a very precise holding (or breakdown) voltage as that value of drain voltage at which the transistor will just be able to turn off, when swept from positive to negative gate voltage, as shown in Fig.1 for $V_D = 5.3V$. This paper describes how simulation has been used to both quantify and explain the dependence of breakdown voltage on key parameters such as gate length, oxide thickness and SOI film doping.

2. Simulation details

The simulations of breakdown have been carried out using a modified version of MINIMOS4[3], which has been adapted to include bandgap narrowing and a non-local 'lucky electron' impact ionisation model[4]. This model, which also incorporates an energy dependent electron mean free path requires no fitting parameters and yet provides accurate estimates of substrate current for sub-micron bulk silicon transistors, both with and without a lightly doped drain[5]. By evaluating the individual components of current flow, it is possible to use the simulator to derive an effective value for the equivalent bipolar current gain[6], an extremely useful parameter in interpreting the contribution of minority carrier injection at the source junction in lowering the breakdown voltage. A fixed value of carrier lifetime of 0.1 microseconds was used in all simulations.

An initial validation of the accuracy of the simulator is illustrated in Fig.2, which compares measured and simulated bipolar holding voltage as a function of gate length. A reduction in holding voltage occurs because of an increase in bipolar current gain due to reduced base width (gate length). The effect of reduced gate length on bipolar current gain, (calculated at $V_D = V_h$), is shown in Fig.3, along with the corresponding *reduction* in lateral electric field. This reduction in field at $V_D = V_h$ is a consequence of the condition that the product of current gain and ionisation rate tends to unity at the onset of snapback, so that snapback is triggered at a lower field for shorter gate lengths.

The simulated dependence of holding voltage on SOI film thickness is shown in Fig.4, for two gate lengths. As the film thickness is reduced, current crowding causes a reduction in bipolar current gain, as shown in Fig.5. Despite this reduction in gain, the corresponding increase in the lateral electric field however has a dominant effect on the impact ionisation rate, due to its non-linear dependence on electric field.
Fig.6 shows the effect of reducing gate length for three different film thicknesses. In each case the film doping was chosen to give a threshold voltage of 0.6V. Clearly for short gate lengths, the three graphs tend to converge. The reduction in the relative change in holding voltage as the gate length is reduced from 2μm to 0.5μm is a result of body charging effects. In the thick film device, the film is partially depleted, so that all charge accumulates within the film and as the gate length reduces, the increase in the electric field has its full effect. However, for the thinnest film of 400Å the film is fully depleted, so that the removal of the potential barrier at the source results in a removal of charge from the film. Therefore, the increasing lateral drain electric field has a more limited effect due to a reduction in body charging.

The simulated dependence of holding voltage on film doping is shown in Fig.7, for an SOI transistor, both with and without a lightly doped drain. Superimposed on this plot is the corresponding measured variation (including an LDD), taken from the published literature[7]. The increase in holding voltage for higher doping is caused by a combination of lower current gain and higher lateral electric field at the drain junction. Negative values of doping correspond to an accumulation mode transistor. Fig.8 shows the expected decrease in bipolar current gain with increased film doping, in agreement with standard bipolar theory. At low doping, high bipolar gain dominates, whilst for high doping, reduction in bipolar gain is compensated by increase in impact ionisation due to higher electric field, so that eventually the holding voltage becomes independent of film doping when only partial as opposed to full depletion of the SOI film occurs.
The pattern shown for the ultra-thin film transistor of Fig.7 differs when the same parameters are used but the film thickness is increased. Fig.9 compares the dependence of thick and thin film transistors, with no lightly doped drain, on film doping. Clearly for the thicker film a clear optimum doping exists to maximise the holding voltage, defined by the boundary between full and partial depletion. An explanation of this dependence may be inferred from Fig.10. Clearly the current gain is more sensitive to film doping for the transistor with the thicker film. In this case, as the film doping is increased from 0 to $3x10^{16}cm^{-3}$, the current gain is reduced by almost two orders of magnitude and this reduction predominates over the increase in electric field, resulting in an increase in holding voltage. For larger values of doping, the current gain reduces much less rapidly, whilst the electric field continues to increase, so that the holding voltage is lowered. In the thin film case however, because the current gain is much less

dependent upon the film doping it is compensated much more by the electric field.

3. Conclusions

Simulation has shown that both reduced gate length and film thickness, result in lower breakdown voltage in an SOI transistor. In the former case, both the current gain and the lateral electric field are increased. In the latter case, however, the dependence of holding voltage on film thickness depends on the relative effects of lower bipolar gain and higher electric field with reduction in film thickness. In fully depleted sub-micron gate transistors the high film doping associated with enhancement mode transistors offers the possibility of low threshold voltage, steep subthreshold slope and high holding voltage.

References

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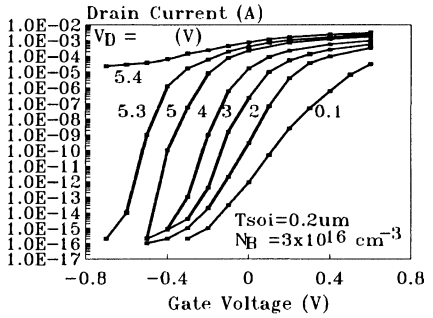

Fig.1 Variation of drain current with gate voltage for a 1μm SOI transistor, T_{OX} = 27nm.

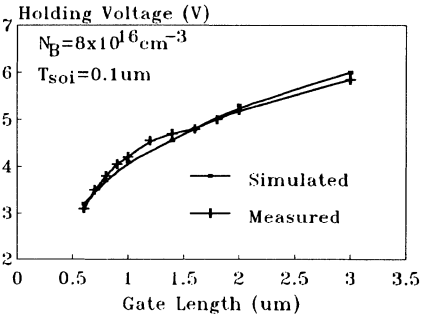

Fig.2 Dependence of holding voltage on gate length for SOI transistors, T_{OX} = 20nm.

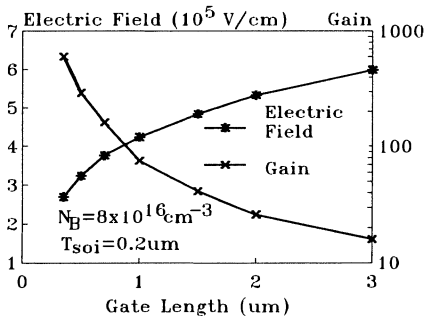

Fig.3 Variation of lateral electric field and current gain, for V_D = Vh, V_G = Vt.

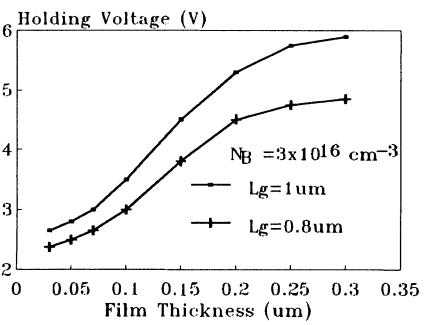

Fig.4 Dependence of holding voltage on film thickness and gate length.

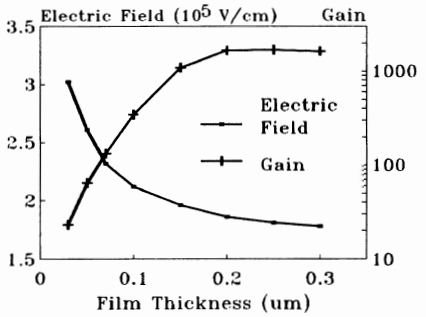

Fig.5 Variation of lateral electric field and current gain at $V_D = 2.5V$ and $V_G = Vt$, for a $1\mu m$ SOI transistor.

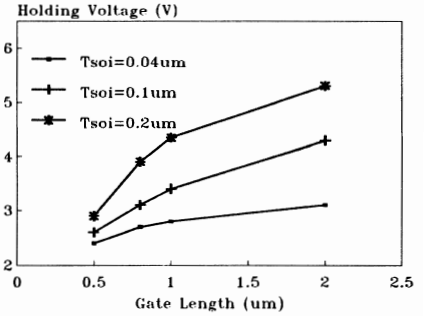

Fig.6 Variation of holding voltage with gate length and film thickness.

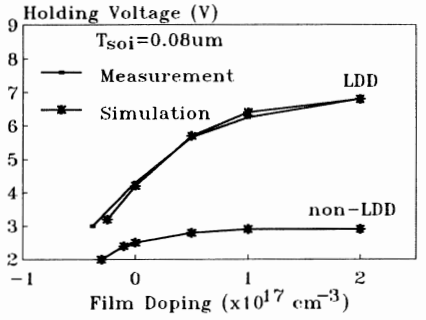

Fig.7 Simulated and measured variation of holding voltage with film doping, $Lg = 0.8\mu m$, $T_{OX} = 15nm$.

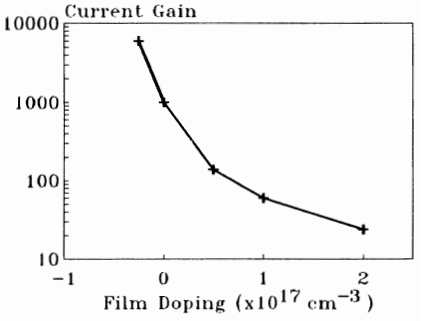

Fig.8 Dependence of current gain on film doping, $V_D = Vh$ and $V_G = Vt$.

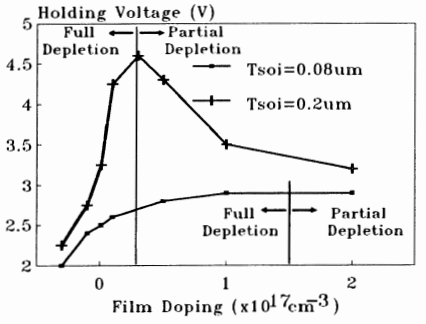

Fig.9 Dependence of holding voltage on film doping.

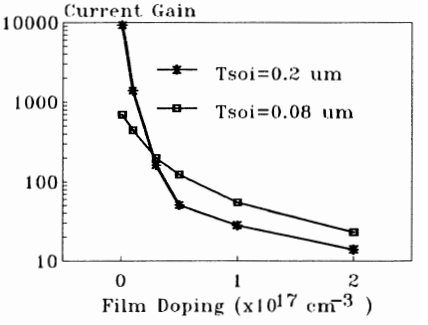

Fig.10 Variation of current gain with film doping, at $V_D = Vh$ and $V_G = Vt$.