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Noise in $Si/Si_{1-x}Ge_x$ n-channel HEMTs and p-channel FETs

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Abstract

A theoretical model to evaluate noise in $SiGe/Si$ based n-channel MODFETs and p-channel MOSFETs is presented. The analysis is based on a self-consistent solution of Schrödinger and Poisson's equations. In this study, n-channel FETs exhibit a better noise performance than that of p-channel FETs. The influence of device parameters on noise properties for this class of devices are presented.

1. Introduction

Noise can be characterized by measuring the minimum noise figure F_{min} or the noise temperature. Extensive experimental and theoretical efforts have been directed to the study of noise figure in III-V HEMTs, however, no such study exists for $SiGe/Si$ based devices. In this paper a noise model is presented which is based on a self-consistent solution of Schrödinger and Poisson's equations [1-3]. The calculation of noise parameters follows the treatment presented by Anwar et. al. [1].

2. Model

The modeling of noise proceeds by first quantifying the quantum well (QW) behavior and identifying a realistic velocity-electric field ($v_d - \mathcal{E}$) characteristic for the carrier in the conducting channel. Instead of using a two-line or an exponential approximation the following $v_d - \mathcal{E}$ [1,3] is used in this calculation, $v_d = v_s\mathcal{E}/\sqrt{(v_s/\mu_0)^2 + \mathcal{E}^2}$, where v_s is the saturation velocity, μ_0 is the low field mobility and $\mathcal{E}$ is the applied electric field along the channel. This $v_d - \mathcal{E}$ characteristic makes the current-voltage and dc small signal parameters analytic in nature [4] and provides a better agreement with results obtained from Monte Carlo simulation. The QW parameters are calculated self-consistently [2] and introduced in the calculation of noise by recognizing the functional dependence of the average distance of the electron cloud x_{av} and the position of the Fermi level E_F on the 2DEG concentration n_s [2].

The analysis of noise is based on the identification of the different noise sources

that are present in the conducting channel, namely (a) Johnson Noise in the ohmic region (unsaturated region), (b) noise associated with spontaneous generation of dipole layers in the saturation region, (c) gate noise due to elementary voltage fluctuations in the channel and (d) induced gate noise in the saturation region. The noise analysis is carried out by accounting for all these noise sources and their correlation coefficients [2]. The minimum noise figure, F_{min}, the noise conductance, g_n, the minimum noise temperature, T_{min}, and the optimized external generator source impedance, $Z_{s,opt}$ can be written as :

$$F_{min} = 1 + 2 \cdot g_n \cdot (R_c + \sqrt{R_c^2 + \frac{r_n}{g_n}}) \tag{1}$$

$$T_{min} = 2 \cdot T \cdot g_n \cdot [R_c + Z_{s,opt}] \tag{2}$$

$$g_n = g_m \cdot (\frac{f}{f_T})^2 \cdot [P + R - 2C\sqrt{PR}] \tag{3}$$

$$Z_{s,opt} = \sqrt{R_c^2 + \frac{r_n}{g_n}} \tag{4}$$

where r_n is noise resistance defined in Ref.[1], $Z_c = R_c + jX_c$, is the correlation impedance, R_s and R_g are the source and drain impedance, $R_i = \frac{L_g}{v_s C_{gs}}$, is the gate charging resistance. L_g represents the length of the gate. In several cases, the device is not matched for the minimum noise figure and the mismatch effect on the noise figure can be expressed as

$$F = F_{min} + \frac{g_n}{R_s} \cdot |Z_s - Z_{s,opt}|^2 \tag{5}$$

where $Z_s = R_s + jX_s$ the input termination, or source, impedance. Eqn. (5) shows that the mismatch effect is less sensitive for lower values of the noise conductance g_n.

3. Results and Discussion

In this paper, the n- and p-channel devices analyzed are based on the structures reported in Refs. [5] and [6]. In Fig.1, the calculated minimum noise figure, F_{min} (dB), is plotted as a function of the drain-source current for n- and p-channel FETs with temperature as a parameter. The calculations are performed at 15 GHz. The present noise model predicts "U" shape in minimum noise figure (F_{min}) versus saturation drain current I_{ds}. The minimum noise figure of n-channel devices are smaller than that of p-channel devices at both temperatures. At higher I_{ds}, the increase of noise figure for p-channel devices is faster than that of n-channel device. This may be due to the fact that n-channel FETs have higher transconductance g_m and unity current gain cut-off frequency f_T than those of p-channel FETs [4].

In Fig.2, F_{min} is plotted as a function of frequency for n- and p-channel FETs at various temperatures. For the p-channel MOSFET V_{gs} = -2.5V (-1.64V) and V_{ds} = -2.5V at 300K (82K), for the n-channel MODFET V_{gs} = -0.65V (-0.53V) and V_{ds} = 3.0V at 300K (77K). F_{min} increases with frequency for both families of FETs. A higher f_T for n-channel MODFETs results in a lower F_{min}. We have observed that F_{min} decreases with increasing QW width. This decrease in not so significant at the high frequency end. At 60 GHz a well width increase from 50Å to 300Å may result

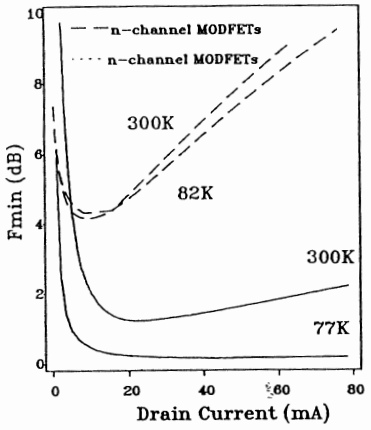

Fig.1 Minimum noise figure F_{min} is plotted as a function of drain current for $SiGe/Si$ based n- and p-channel FETs with temperature as a parameter.

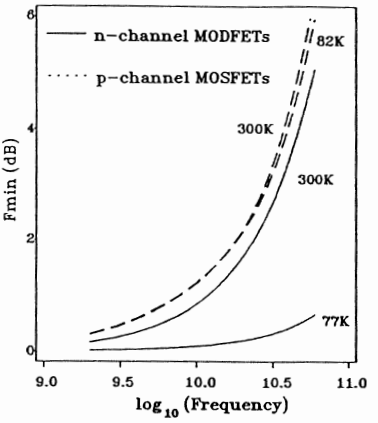

Fig.2 Minimum noise figure F_{min} is plotted as a function of frequency for both n- and p-channel FETs with temperature as a parameter.

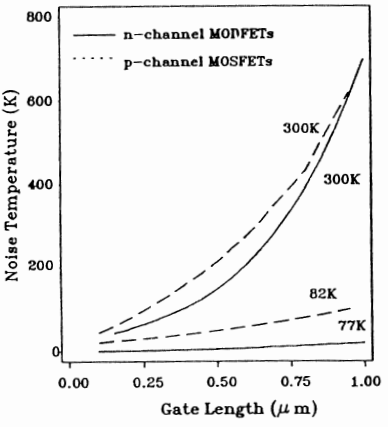

Fig.3 Minimum noise temperature T_{min} is plotted as a function of gate length for both n- and p-channel FETs with temperature as a parameter.

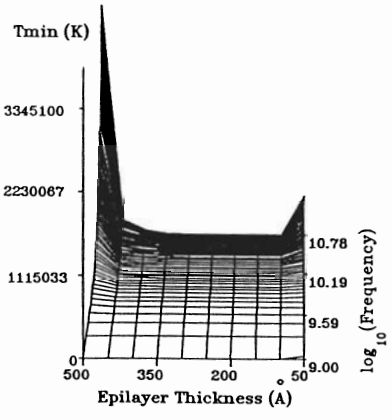

Fig.4 Minimum noise temperature T_{min} is plotted as a function of the doped epilayer thickness for an n-channel FET at 77K.

in a reduction of F_{min} by 1.5dB for n-channel FETs. F_{min} is less sensitive to QW width variation at cryogenic temperatures.

In Fig.3, minimum noise temperature T_{min} is plotted as a function of gate length for both n- and p-channel devices with temperature as a parameter. Noise temperature increases with increasing gate length for both devices. For a given drain-source voltage, the thermal noise induced from ohmic region will increase by increasing gate length (also increasing the length of ohmic region). Therefore, noise will increase by increasing gate length for both n- and p-channel devices.

In Fig.4, T_{min} is plotted as a function of the doped epilayer thickness (d_d) and frequency for an n-channel FET at 77K. As observed, a range of d_d exists (75Å-200Å) where T_{min} is a minimum ($T_{min} < 200$K at 60 GHz for 75Å$\leq d_d \leq$ 200Å). The reduction in T_{min} is prominent at higher frequencies. For p-channel devices T_{min} increases slightly with increasing d_d.

Based on the present noise model, it is observed that the calculated noise parameters are less sensitive to the donor concentration than those of the conventional $AlGaAs/GaAs$ based FETs.

4. Conclusion

A self-consistent model to calculate F_{min} and T_{min} in $SiGe/Si$ n-channel MODFETs and p-channel MOSFETs is presented. These predictions of noise parameters may lead one to optimize the noise performance for $SiGe/Si$ based FETs.

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