SIMULATION OF SEMICONDUCTOR DEVICES AND PROCESSES Vol. 5
Edited by S. Selberherr, H. Stippel, E. Strasser – September 1993

Physical IGBT Model for Circuit Simulations

M. Andersson, M. Grönlund, and P. Kuivalainen

IC Design, Semiconductor Laboratory, Technical Research Center of Finland
Olarinluoma 9, SF-02200 Espoo, FINLAND

Abstract

An improved analytical model for IGB power transistors has been developed for circuit simulators. Special attention is paid to the physical modeling of the short channel in the DMOS branch and the buffer layer near the anode in IGBT device structures. Good agreement between simulated and measured data has been obtained.

1. Introduction

Recent advances in power and high-voltage integrated circuits have allowed the integration of new emerging power devices with high performance MOS logic. One of the most promising power devices in terms of integration possibilities is the lateral insulated gate bipolar transistor (LIGBT) [1]. Recently, the integration of a vertical IGBT with a control circuit has been demonstrated [2]. The IGBT's have unique electrical characteristics which combine the low on-state resistance of the bipolar power transistor and the low driving power requirements of the MOS gate.

Computer-aided design of analog circuits including power IGBT's is critically dependent on reliable device models implemented in circuit simulators, e.g. SPICE. Due to deficient MOSFET and BJT models in SPICE, simulations in which these conventional power device models are used to describe new devices cannot accurately account for the special features of these new devices. In the present work we have developed a physical IGBT model for circuit simulations to overcome this problem. Special attention is paid to the modeling of the DMOS channel region and the n^+-buffer layer close to the pnp-emitter region. In the previously published IGBT models [3-5] for circuit simulations, the treatment of these regions has been neglected. In the MOS channel region model, mobility degradation due to high electric fields and the effect of doping gradient on the threshold voltage are taken into account. For the low gain, high injection bipolar pnp-transistor part of the IGBT structure, ambipolar transport theory is applied, extending the treatment to the case of a heavily doped buffer layer close to emitter.

2. Model

The basic structure of a vertical IGBT having a n+-buffer is shown in Fig. 1. The wide base pnp bipolar branch is driven by an enhancement-type n-MOSFET. With a positive gate voltage the electrons flow towards the anode through the inverted surface channel in the p-well. In the forward conduction mode the anode (or drain) injects minority carriers (holes) through a buffer layer into the lightly doped n-type base. This injection greatly enhances the conductivity of the wide base region, which in turn results in an additional lowering of the on-state resistance.

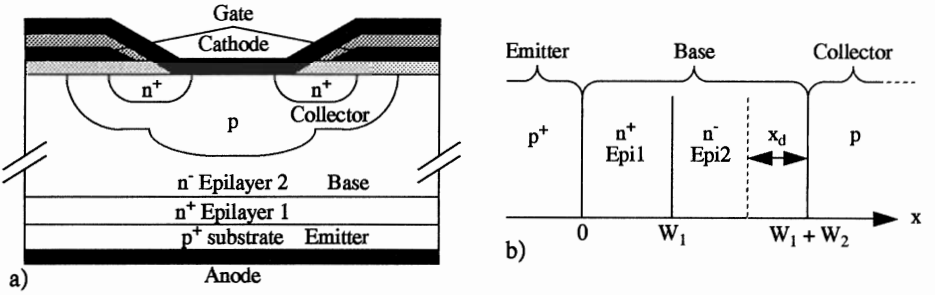

Figure 1. (a) Cross-section of a vertical IGBT. (b) Coordinate system used in the model.

2.1 Buffered wide base BJT model

We now extend the previously published [3-5] physical model equations for the pnp BJT by taking into account the buffer layer close to the emitter (anode), Fig. 1. This layer has been added to the IGBT structure since it increases the forward punch-through voltage and speeds up the turn-off process. The latch-up resistance is also improved by the buffer layer.

Base transport is described by the ambipolar transport equation in both epilayers of the base

$$\frac{d^2 p_i(x)}{dx^2} - \frac{1}{L_{pi}^2} \cdot p_i(x) = 0 \tag{1}$$

where $L_{pi} = \sqrt{D_{Ai}\tau_{Hi}}$ is the ambipolar diffusion length and the index i(=1,2) refers to the epilayer regions shown in Fig. 1 (b). The solution to (1) is a linear combination of exponential functions and the coefficients can be determined from proper boundary conditions obtained from the continuity of the hole current and concentration at W_1. Furthermore, we know that $p_2(x=W_1+W_2-x_d) = 0$, at the end of the neutral base region near the base-collector junction, since this junction is always reverse biased. Applying these boundary conditions we obtain the one-dimensional hole distribution from (1)

$$p_i(x) = \frac{p(0)}{A}\left[\cosh\left(\frac{x-W_1}{L_{pi}}\right) - \left(\frac{D_{A2}L_{p1}}{D_{A1}L_{p2}}\right)^{2-i} \coth\left(\frac{W_2 - x_d}{L_{p2}}\right)\sinh\left(\frac{x-W_1}{L_{pi}}\right)\right] \tag{2}$$

with

$$A = \frac{D_{A2}L_{p1}}{D_{A1}L_{p2}}\coth\left(\frac{W_2 - x_d}{L_{p2}}\right)\sinh\left(\frac{W_1}{L_{p1}}\right) + \cosh\left(\frac{W_1}{L_{p1}}\right) \tag{3}$$

p(0) is the hole density at the edge of the emitter-base (p^+-n^+) junction space charge region, and by using the quasi-equilibrium assumption it can be expressed in terms of the emitter-base-voltage V_{EB}, $p(0) = [n_i^2/N_{epi1}] \exp(qV_{EB}/k_B T)$. x_d is the depletion region width of the collector-base junction.

With the aid of the hole densities (2), the emitter and base current densities can be expressed as

$$J_E = \frac{b+1}{b}\left\{J_{no}\left[\frac{p_1(0)}{n_i}\right]^2 - qD_A\frac{dp_1}{dx}(x=0)\right\} \tag{4}$$

$$J_B = J_{no}\left[\frac{p_1(0)}{n_i}\right]^2 + q\int_0^{W_1}\frac{p_1(x)\,dx}{\tau_{H1}} + q\int_{W_1}^{W_1+W_2-x_d}\frac{p_2(x)\,dx}{\tau_{H2}} \tag{5}$$

where J_{no} is the saturation current density that defines the back injection of electrons into the emitter region, b the ratio between the electron and hole mobilities, and τ_{Hi} (i=1,2) is the high injection carrier life-time. The collector current density J_C is expressed as J_E-J_B. By using the hole and current densities (2) - (5) the voltage drop in the neutral base region can be calculated as in [3].

Finally, in the transient modeling of the IGBT [3], we need the depletion charge density at the base collector junction $Q_{BC} = qA_C N_{epi2} x_d$, and the base charge

$$Q_B = qA_E\int_0^{W_{M1}} p_1(x)\,dx + qA_E\int_{W_1}^{W_{M2}} p_2(x)\,dx \tag{6}$$

where W_{Mi} is the point where $p_i(x)$ is equal to the doping density in the epilayer i.

2.2 Channel region model

A physical channel region model for IGBT has been modified from the SPICE level 3 MOSFET model (MOS3)[6]. The modifications include an improved treatment of charge carrier mobility degradation phenomena according to experimental measurements and the effect of the doping concentration gradient on the threshold voltage. The final equations are the same as in MOS3 model excluding the effective mobility expression μ_{eff} and the threshold voltage V_{TH}:

$$\mu_{eff} = \frac{\mu_s}{\left[1 + \left(\frac{V_{DS}\mu_s}{VMAX \cdot L}\right)^p\right]^{1/p}} \tag{7}$$

$$V_{TH} = V_{FB} + PHI + \frac{2}{\eta}\left(1 - e^{-\eta/2}\right)\left(GAMMA \cdot F_S\sqrt{PHI}\right) \tag{8}$$

Here the model parameters are the same as in the original MOS3 model excluding a new parameter p which is related to the electric field dependence of the carrier velocity and the parameter η for the doping concentration gradient. An exponential position dependence was

assumed for the acceptor doping in the channel region of a n-type DMOS structure, $N_A(x)=N^0_A\exp(-\eta x/L)$. The new parameter p improves the accuracy of the model and it allows the use of a physical value for the saturation velocity parameter VMAX. Our modified MOSFET model reduces to the SPICE MOS model in the case $\eta=0$ and $p=1$.

3. Simulation results

The device physics based IGBT model, which suits both lateral and vertical structures, has been implemented in the APLAC circuit simulator [6]. An advantage of the APLAC is that it provides optimization capabilities for the model parameter extraction. Fig.2 (a) compares the results from the simulations and the measurements of the dc electrical characteristics of a lateral IGBT fabricated in our laboratory. Fig. 2 (b) shows the transient behaviour of the same device. In both cases the agreement between the simulations results and the measured data is good.

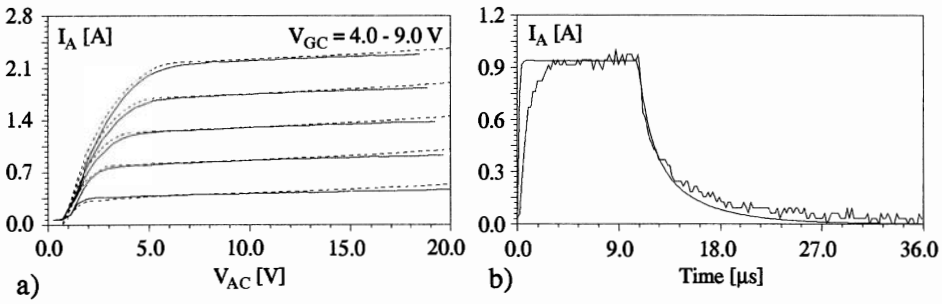

Figure 2. (a) Measured and simulated (dotted lines) LIGBT anode current versus anode voltage for gate voltages in the range 5.0-9.0 V. (b) Measured and simulated current versus time for turn-on and turn-off transients in a LIGBT. Risetime discrepancy is due to unknown parasitic inductance. The LIGBT has been processed in our laboratory, and its gate dimensions are W/L = 0.03 m / 8 µm.

References

[1] M.N.Darwish, M.A.Shibib, *Lateral MOS-Gated Power Devices- A Unified View*, IEEE Trans.Electron Dev. 38 (1991) 1600.

[2] T.Mizoguchi, T.Shirasawa, M.Mori, Y.Sugawara, *600 V, 25 A Dielectrically-Isolated Power IC with Vertical IGBT*, IEEE Proceedings of the 3rd International Symposium on Power Semiconductor Devices and ICs, 1991, 40.

[3] J.G.Fossum, R.J.McDonald, M.A.Shibib, *Network Representations of LIGBT Structures for CAD of Power Integrated Circuits*, IEEE Trans. Electron Dev. 35 (1988) 507.

[4] S.Eränen, M.Grönlund, M.Blomberg, J.Kiihamäki, *The Kirk Effect in the LIGBT Devices*, IEEE Trans.Electron Dev. 38 (1991) 1919.

[5] Z.Shen, T.P.Chow, *An Analytical IGBT Model for Power Circuit Simulation*, IEEE Proceedings of the 3rd International Symposium on Power Semiconductor Devices and ICs, 1991, 79.

[6] M. Valtonen et al., Helsinki University of Technology, Circuit Theory Laboratory & Nokia Research Center, Hardware Design Technology, *APLAC, An Object-Oriented Analog Circuit Simulator and Design Tool*, 6.1 User's Manual & 6.1 Reference Manual, December 1992.