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Multivariable Optimization of Planar Junction Termination with Respect to Technological Tolerances

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Abstract

A procedure for the multivariable optimization of device properties regarding feasible technological tolerances in the fabrication process is presented. It is applied to a planar junction termination technique. By optimizing the lateral doping profile the allowed fabrication tolerance for a 1.4 kV junction termination could be substantially enhanced.

1 Introduction

Device optimization by theoretical and computational means is the main objective of simulation of semiconductor devices and processes. Most optimization studies are based on the variation of individual parameters, thereby leaving the choice of a promising way of variation to the genius of human brain. Though this is certainly not the worst way, there should be more economic possibilities for arriving at an optimal design, especially if the space of variable parameters is multidimensional. An example of a multivariable procedure has been given by Waddell et al. [1], who minimized the surface electric field of two different junction termination structures.

A second goal of device optimization is to increase fabrication yields. This aspect often has been neglected since high yield and optimal device properties seem to exclude each other.

The intention of the present investigation is to show a way of optimizing device properties depending on several parameters regarding a given technological tolerance in the fabrication process.

The optimization procedure is applied to the method of planar junction termination by variation of the lateral doping profile (VLD) [2—6].The critical technological parameter in this case is the depth of etching of the VLD-region, which is used to adjust the total charge of this region to the required value.

2 Planar Junction Termination Method

The fabrication process of the VLD-structure has been described elsewhere [3, 5, 6]. Let us therefore concentrate on the two essential ingredients. We start at the doping profile of the VLD-region sketched in Figure 1a. The concentration of the p-doped (Al) layer is decreasing

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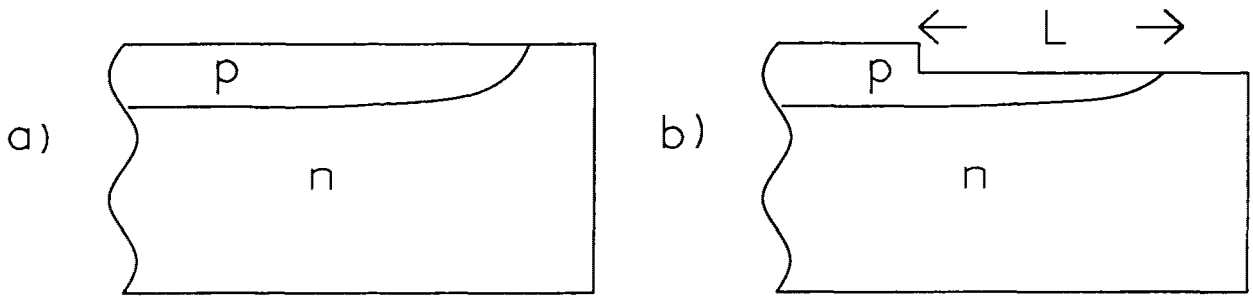

Figure 1: Planar junction termination a) before and b) after etching process

towards the edge of the device, starting at a relatively high value required e.g. for the p-base of a GTO-thyristor. The doping profile can be calculated by means of process simulation or approximated to a good accuracy by the product ansatz

$$N_A(x,y) = N_l(x)\, N_v(y) \tag{1}$$

Here $N_v(y)$ is the vertical profile produced by a one-dimensional Al-diffusion process, $N_l(x)$ descibes the relative decrease of doping in lateral direction.

The last fabrication step consists of a depletion etch (Figure 1b). The depth of etching is a technologically critical parameter since the ratio of dopant dose after etching to dopant dose before etching is rather small (in the case presented here $\sim 1/100$).

The function $N_l(x)$ determines the breakdown voltage at a given depth of etching. The aim of the optimization is to find the best $N_l(x)$, which is defined as to ensure the highest breakdown voltage in the interior of an interval of given size of the depth of etching.

3 Optimization Procedure

Breakdown voltage is calculated by means of the two-dimensional poisson solver BREAKDOWN [7, 8] in the ionisation integral approximation. The ionisation integrals for holes

$$\Phi_p = \int_0^w \alpha_p(s) \exp\left\{ - \int_0^s \left[\alpha_p(s') - \alpha_n(s')\right] ds' \right\} ds \tag{2}$$

are calculated along electric field lines. Breakdown occurs when the maximum of the ionisation integrals reaches the value 1. We use the ionisation coefficients by van Overstraeten and de Man [9].

A crucial point in nonlinear optimization problems is the choice of the set of optimization parameters since a bad choice can lead to severe problems with convergence and will at least substantially enhance the expenditure of CPU-time. A good set should be in a sense orthogonal.

We therefore did not define the lateral profile $N_l(x)$ point by point but used the following definition

$$N_l(x) = \cos\left[\frac{\pi}{2}P(x)\right] \tag{3}$$

with

$$P(x) = P_1(x) + \sum_{i=2}^{n} \alpha_i T_i\left(\frac{2x}{L} - 1\right) \tag{4}$$

The α_i are the optimization parameters (α_1 is the absolute location of the etching interval), T_i are Chebyshev polynomials, and $P_1(x)$ is a linear function which makes $P(0) = 0$ and $P(L) = 1$. Negative concentrations are replaced by zero. The number of optimization parameters is n. The cosine serves to provide an upper limit for the doping concentration.

The optimization problem can now be formulated in the following way: Maximize the voltage across the device under the constraints that the ionisation integrals through all points of interest at any depth within the etching interval be less or equal to 1. Further constraints may be included such as an upper limit of the surface electric field or of the lateral extension of the space charge region.

As an approximation to this a certain number (usually 5) of points within the etching interval were taken into account. It is not sufficient however to choose the two end points of the interval only.

The optimization procedure is broken up into a sequence of single steps, each of which consists of a linear programming problem: First the breakdown voltage is calculated for a given set of parameters $\alpha_1^{(0)}, \ldots, \alpha_n^{(0)}$. At this voltage the ionisation integrals and their derivatives with respect to the optimization parameters are calculated. The ionisation integrals (or rather their logarithms) are approximated by their first-order Taylor series

$$\Phi_p(\alpha_1, \ldots, \alpha_n) = \Phi_p(\alpha_1^{(0)}, \ldots, \alpha_n^{(0)}) + \sum_{i=1}^{n} \frac{\partial \Phi_p}{\partial \alpha_i}(\alpha_i - \alpha_i^{(0)}) \tag{5}$$

This is also done for possible further constraints (note that the numerical calculation of the derivatives is not so expensive as one might expect since the SOR-algorithm used in BREAKDOWN can start from a good approximation to the solution).

With the linearized dependencies of the ionisation integrals a linear program is defined: Minimize the maximum of all ionisation integrals (with the constraint that all other ionisation integrals may not be greater) at the given voltage. Additional constraints concerning the size of the changes of the parameters are put in in order not to leave the realm of equation (5). This problem is solved using a standard SIMPLEX routine. The result is a new set of parameters with (in general) a higher breakdown voltage.

4 Results

As an example the application of the optimization procedure to a structure with the following parameters is shown: substrate doping 2 x 10^{13} cm^{-3}, maximum doping of p-region 8 x 10^{16} cm^{-3}, depth of pn-junction 70 μm, length of the VLD-region 2.5 mm. The size of the etching interval is taken to be 6 μm. The calculated bulk breakdown occurs at 5110 Volt. The number of optimization parameters is limited to 6 in this example.

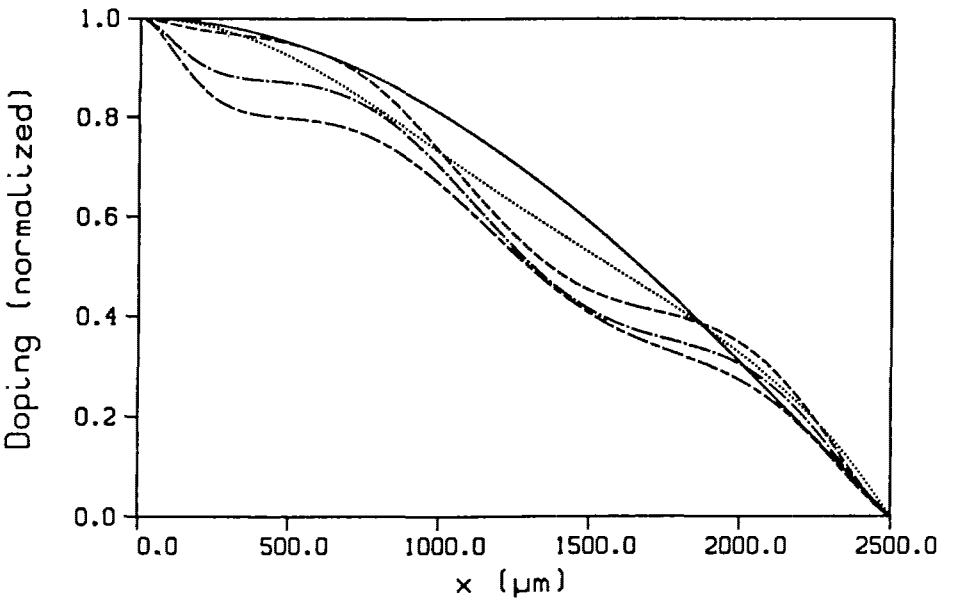

Figure 2: Lateral doping profile at different stages of the optimization (see text)

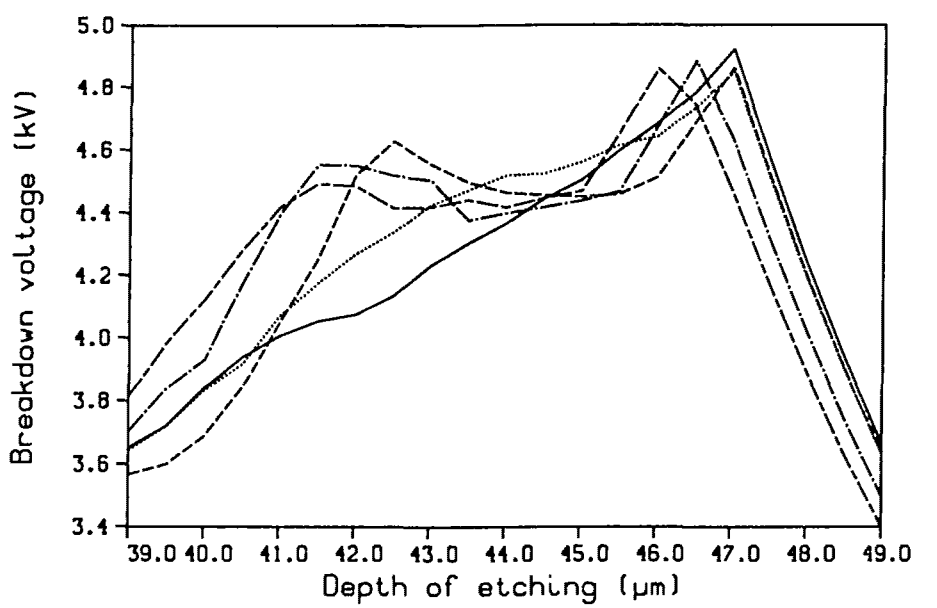

Figure 3: Dependence of the breakdown voltage on the depth of etching at different stages of the optimization

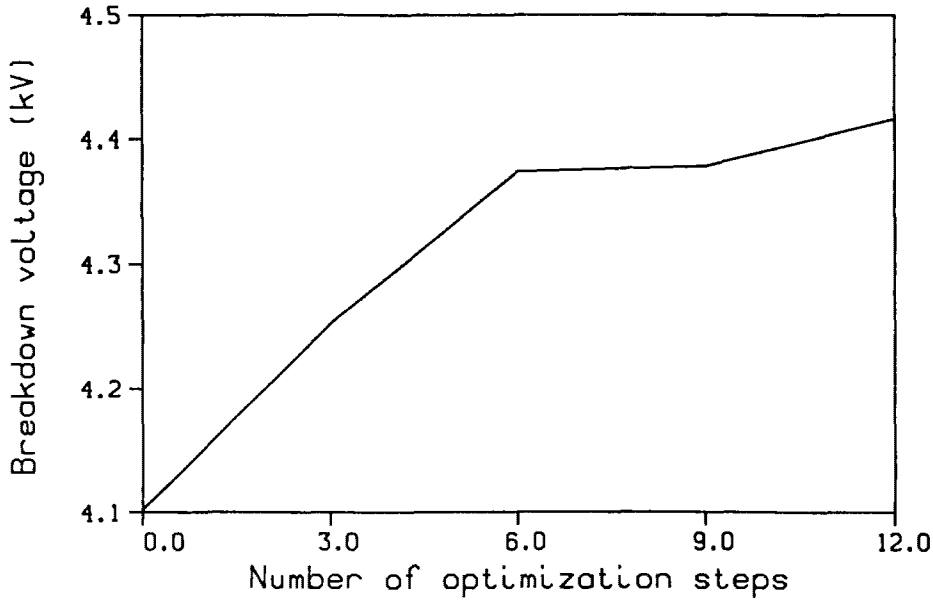

Figure 4: Minimum breakdown voltage within the 6 μm interval of the depth of etching as function of the number of optimization steps

The optimization starts with a lateral profile corresponding to $\alpha_i = 0$ $(i \geq 2)$ in equation (4) (full line in Figure 2). The breakdown voltage for this profile as a function of the depth of etching is given as the full line in Figure 3. The profiles after 3 (dotted line), 6 (dashed line), 9 (chain-dotted line), and 12 (chain-dashed line) steps of optimization, respectively, are also shown in Figure 2. Figure 3 additionally contains the corresponding breakdown voltage vs. depth of etching curves.

The minimum breakdown voltage within the interval of etching increases from 4.1 kV to more than 4.4 kV (Figure 4). From Figure 3 it can be seen that the allowed size of the interval of etching necessary for a 4.4 kV junction termination is enhanced from 3.6 μm before the optimization to 6.2 μm after 12 steps of optimization.

Figure 5 shows the maximum value of the surface electric field as a function of the depth of etching (after optimization). The maximum electric field is rather low compared to other techniques of junction termination, although it was not included in the optimization process. This is due to the rather large length of the VLD-region. In case the length of the VLD-region is smaller it might be advisable to put an upper limit for the surface electric field as a constraint into the optimization procedure as described above.

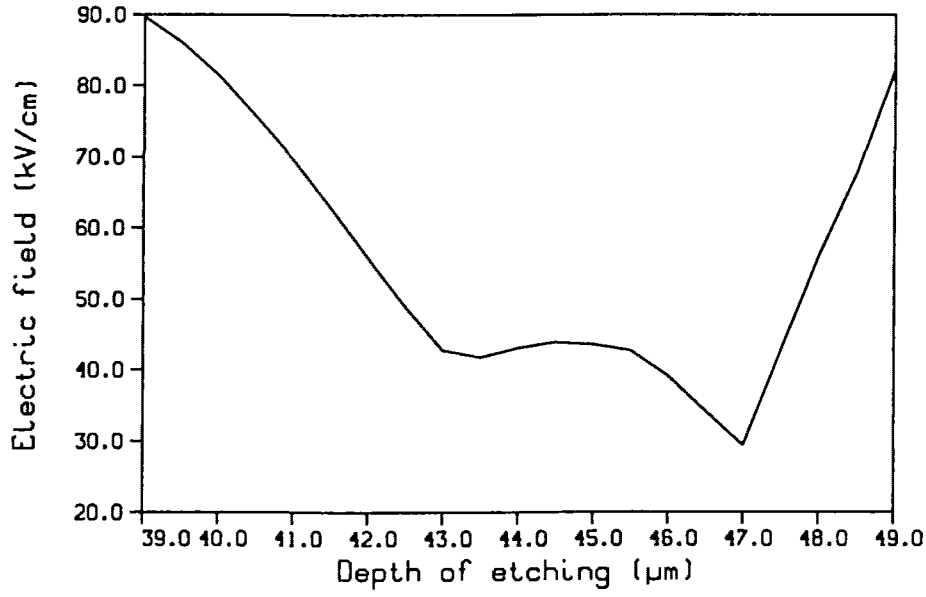

Figure 5: Maximum surface electric field vs. depth of etching after 12 steps of optimization

5 Conclusions

We have presented a procedure for the multivariable optimization of device properties regarding technological tolerances in the fabrication process. The application to a planar junction termination technique has shown that using a procedure of this kind it is possible to arrive at considerable improvements concerning either the fabrication yield (for a given specification of the device) or the properties of the device (for a given technological tolerance).

There are however a number of important points for the efficiency of an optimization procedure based on a device simulation program:

- Optimization parameters should be in a sense orthogonal. Otherwise the convergence properties can be strongly deteriorated. In the example given here the parameters meet this condition reasonably well with the exception of the depth of etching. The consequence can be seen from Figure 4: After six optimization steps improvements are rather small whereas the parameters still change considerably.

- Interference between optimization and numerical artefacts in the device simulation should be avoided. This means that the dependence of the grid on the optimization parameters must not destroy the differentiable dependence of the device properties on the parameters. Furthermore it does not make sense to optimize to a better accuracy than the one given by the discretization error of the underlying simulation program.

- In the numerical calculation of derivatives CPU-time can be saved by starting from a good approximation to the solution. If at some point within the technological tolerance there is no danger of violating the constraints it is not necessary to evaluate the derivatives.

- It is desirable to have a good estimate of the "best" limit of parameter changes. This means to get information about the degree of nonlinearity of the optimization problem.
- The way technological tolerances are included here seems to be somewhat crude. Especially if more than one parameter is subject to large variation the computational effort will be very high. Therefore a more economic approach is needed for problems of greater complexity.

In the future device optimization under consideration of feasible technological tolerances will be a challenging task. For the fully automatic solution of complex problems of this kind still a great effort has to be made.

Acknowledgement

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References

[1] J. B. Waddell, J. Middleton, and K. Board: A Design Model for Surface-Termination Optimization of Off-State Semiconductor Devices, IEEE Trans. **ED 36** (1989), 943-953

[2] R. Stengl, U. Gösele, C. Fellinger, M. Beyer, and S. Walesch: Variation of Lateral Doping as a Field Terminator for High-Voltage Power Devices, IEEE Trans. **ED 33** (1986), 426-428

[3] H. J. Schulze and R. Kuhnert: Realization of a High-Voltage Planar Junction Termination for Power Devices, Solid State Electronics **32** (1989), 175-176

[4] T. Stockmeier and P. Roggwiller: Novel Planar Junction Termination Technique for High Voltage Power Devices, Proc. ISPSD'90, Tokyo (1990), 236-239

[5] H. J. Schulze, J. Sack, F. Pfirsch, C. Boit, and H. Mitlehner: 8kV Thyristors with Improved Electrical Data, PEMC'90 Conference Record (1990), 246-249

[6] H. Mitlehner, F. Pfirsch, and H. J. Schulze: A Novel 8 kV Light-Triggered Thyristor with Overvoltage Self Protection, Proc. ISPSD'90, Tokyo (1990), 289-294

[7] J. Pelka: Untersuchung spezieller Randkonturen hochsperrender p^+n-Übergänge zur Vermeidung von Oberflächendurchbrüchen, Thesis TU Berlin (1983)

[8] E. Falck and W. Gerlach: Berechnung der Durchbruchspannung von planaren pn-Übergängen mit mehrstufigen Feldplatten, AEÜ, Band **43**, Heft 5 (1989), 328-334

[9] R. van Overstraeten and H. de Man: Measurement of the Ionization Rates in Diffused Silicon pn-Junctions, Solid State Electronics **13** (1970), 583-608