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Physical Modeling of Submicron MOSFET's by Using a Modified SPICE MOS3 Model: Application to 0.5 μm LDD MOSFET's

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Abstract

Restoring some of the device physics which was previously eliminated in the original SPICE MOS3 model as a consequence of the crude approximations improves the agreement with measured data for submicron MOSFET's significantly. The MOS3 modifications include an improved treatment of the mobility degradation phenomena and an improved approximation for the saturation voltage. These modifications can readily be implemented in the source code of IC simulator programs which provide the MOS3 model.

1. Introduction

In the submicron regime the dependence of MOS transistor saturation and threshold voltages and charge carrier mobility on the channel length is emphasized. An advantage of the SPICE MOS3 model in IC simulations is its ability to accommodate the various short channel effects [1]. Practically, however, MOS3 suffers from poor agreement with experimental data [2]. We have found that especially in the submicron regime MOS3 could not provide reasonable agreement with the measured data. Furthermore, in the best fits the values of some SPICE parameters such as the saturation velocity VMAX were not physically acceptable. This is a serious problem for the development of consistent dc and transit time models for MOS transistors. As shown recently by McMacken and Chamberlain [3], a physical value of VMAX has to be used in the transit time models for circuit simulators, otherwise the predicted transit time remains too small for short channel MOSFET's.

Wong and Salama [2] have shown that the simplified treatment of mobility degradation in the triode region is a major source of error in the MOS3 model. In the present report we introduce simple modifications to the model by treating the mobility degradation $\mu(E)$ due to

a large horizontal electric field E in the submicron MOS transistor channel in accordance with an experimental μ-E relationship. Also a new expression for the saturation voltage is derived, which differs significantly from previous MOS3 expression in the submicron regime. These simple modifications which result in excellent matching between the measured data and the calculated electrical dc characteristics, can easily be implemented by SPICE users thereby permitting accurate simulation of submicron MOSFETs without increasing the computational time of the MOS3 model.

2. Theory

Experimental measurements of charge carrier drift velocity v(E) have led to the following expression [4]

$$v(x,|\bar{E}|) = \frac{\mu_s|\bar{E}(x)|}{\left[1+\left(\frac{\mu_s|\bar{E}(x)|}{VMAX}\right)^p\right]^{1/p}} \tag{1}$$

where μ_s is the gate modulated surface mobility, and p typically varies between the values 1 and 2. In MOS3 (as also in all other analytic MOS transistor models for IC simulators) expression (1) has been employed with p = 1. This is due to the fact that integrations in the dc current expressions cannot be carried out in closed form by using (1) with p > 1. By using the 2D device simulator MINIMOS we found, however, that in the linear region of the MOSFET operation the electric field is approximately constant and equal to V_{DS}/L, where L is the channel length. This readily allows the derivation of the current-voltage equation

$$I_{DS} = \frac{W}{L}\mu_{eff}C_{ox}\left[V_{GS}-V_{TH}-\frac{1+F_B}{2}V_{DS}\right]V_{DS} \tag{2}$$

with

$$\mu_{eff} = \frac{\mu_s}{\left[1+\left(\frac{\mu_s V_{DS}}{VMAX\cdot L}\right)^p\right]^{1/p}} \tag{3}$$

Here, W is the gate width of the MOS transistor, C_{ox} the gate oxide capacitance per unit area, V_{DS},V_{GS} and V_{TH} are the drain-source, gate-source and threshold voltages, respectively, and

F_B a technological constant [1]. For the case p=1 expression (2) reduces to the original MOS3 drain-source current equation.

In the derivation of the expression for the saturation voltage V_{DSAT} in MOS3, the denominator in (1) has previously been totally neglected [1]. This is equivalent to an approximation stating that the mobility μ is constant when $V_{DS} < V_{DSAT}$ whereafter the carrier velocity is constant, v = VMAX. This approximation, however, results in too small values for V_{DSAT}. In the submicron region the error may be as large as 300 %. We have derived a new expression for V_{DSAT} taking into account the mobility degradation (3), which gives

$$V_{DSAT} = \frac{V_2 - \sqrt{V_2^2 - 4V_1V_3}}{2V_1} \tag{4}$$

where

$$V_1 = (\frac{1}{2} - \frac{1}{p})\,(1+F_B)\,\frac{\mu_s}{L} \tag{5}$$

$$V_2 = (1 - \frac{1}{p})\,\frac{\mu_s}{L}\,(V_{GS} - V_{TH}) + (1+F_B)\,VMAX \tag{6}$$

$$V_3 = (V_{GS} - V_{TH})\,VMAX \tag{7}$$

In order to be able to derive these analytical expressions for V_{DSAT}, we introduced the approximation

$$(1+x^p)^{1/p} \approx 1 + \frac{x}{p} \tag{8}$$

for the denominator in (3). We have estimated the error due to this approximation over the typical electric field range to be 3 - 8 % at most, for the parameter values p = 1.2 - 1.5. Notice that the approximation is used only in the calculation of V_{DSAT}, and not in the calculation of the drain-source current in the triode region.

In the case p = 1, (4) reduces to the ordinary pinch off condition $V_{DSAT} = (V_{GS} - V_{TH})/(1 + F_B)$ for long channel devices, for which $\mu_s/VMAX \cdot L << 1$. In the submicron devices, for which $\mu_s/VMAX \cdot L >> 1$, equation (4) yields

$$V_{DSAT} = \sqrt{\frac{2\mu_s (V_{GS} - V_{TH})}{VMAX \cdot L \cdot (1 + F_B)}} \tag{9}$$

which is exactly the same result as in the BSIM model for MOSFET's (Eq. (A20) in ref.[5]; as in MOS3 the value p = 1 was used also in BSIM).

3. Results

The present enhanced MOS3 model has been implemented in an integrated circuit simulator APLAC [6], which provides MOS3 as a built-in MOS transistor model just as SPICE. An advantage of APLAC is the possibility to extract the device model parameters by using optimization techniques. Figs. 1 and 2 compare the simulated I-V characteristics with the actual measured data for submicron n- and p-channel LDD MOS transistors. The cross section of these devices is shown in Fig. 3 and the fabrication is described in ref. [7]. Current and voltage measurements were carried out on test chip structures using an HP 4145 A Semiconductor Parameter Analyzer controlled from a PC by a measurement program. The agreement between measured and modeled results is very good. We have also tried to simulate these submicron devices using the conventional MOS3 model, but no reasonable agreement could be found with any combination of SPICE parameters. The extracted SPICE parameters for our enhanced MOS3 model are listed in Table I.

Parameter	NMOS	PMOS	UNIT
VTO	0.9	-0.93	V
NSUB	$5 \cdot 10^{16}$	$3 \cdot 10^{16}$	$1/cm^3$
TOX	26.5	26.5	nm
U0	840	217	cm^2/Vs
GAMMA	3.6	1.0	$V^{1/2}$
VMAX	10^5	$6 \cdot 10^4$	m/s
PHI	0.5	0.5	V
XJ	0.1	0.2	µm
THETA	0.13	0.124	V
KAPPA	0.7	1.1	-
ETA	0.01	0.01	-

Table I. Model parameters for enhanced MOS3.

Notice that a physical value for VMAX has been used. We found that increasing the value of the parameter p from 1.0 to 1.35 ... 1.5 improved the fit significantly. In Figs. 1 and 2 a value of 1.5 has been used for p. We have tested our enhanced MOS3 model for various other MOS

technologies by using the same p value of 1.5, and the matching to measured data has also been very good, which shows that p doesn't need to be a user-definable SPICE parameter.

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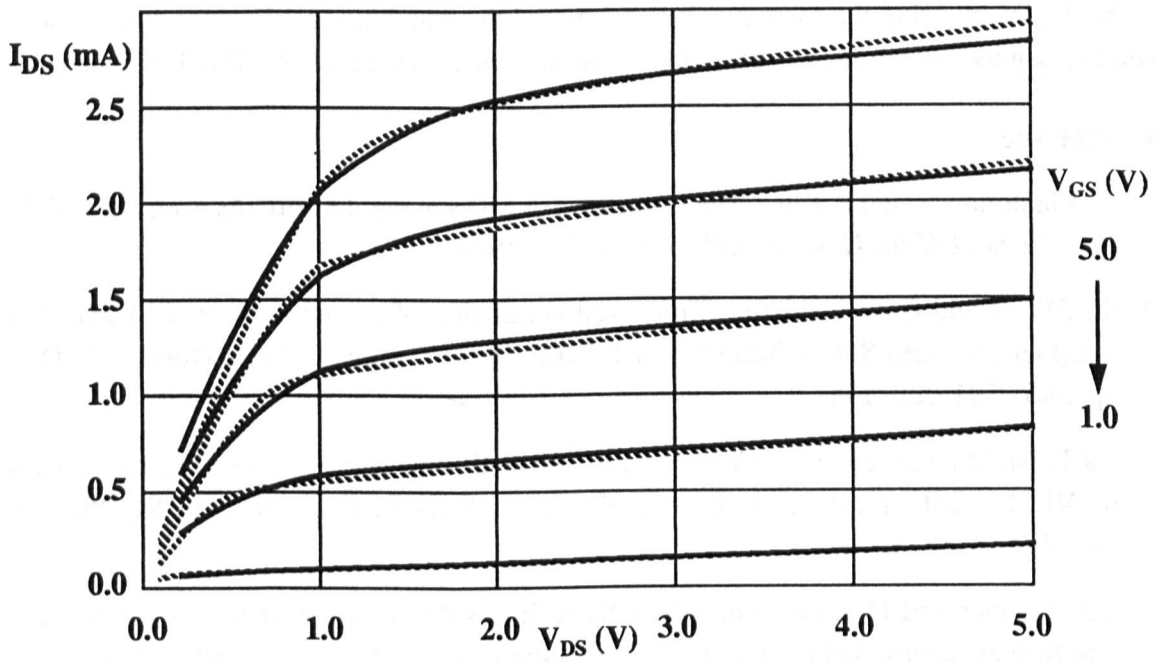

Figure 1. Plot of I-V characteristics comparing the modified MOS3 model simulation results (dotted lines) with measured characteristics (solid lines) for a n-channel LDD MOSFET (W/L = 8.0/0.55 μm).

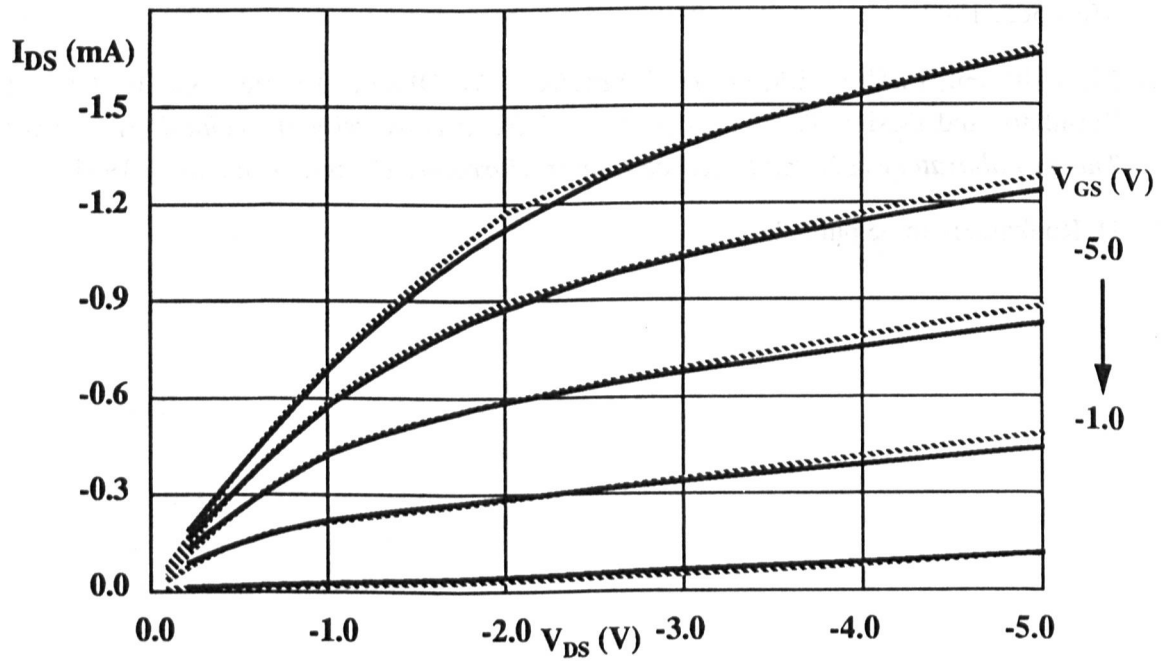

Figure 2. Plot of I-V characteristics comparing the modified MOS3 model simulation results (dotted lines) with measured characteristics (solid lines) for a p-channel LDD MOSFET (W/L = 8.0/0.5 μm).

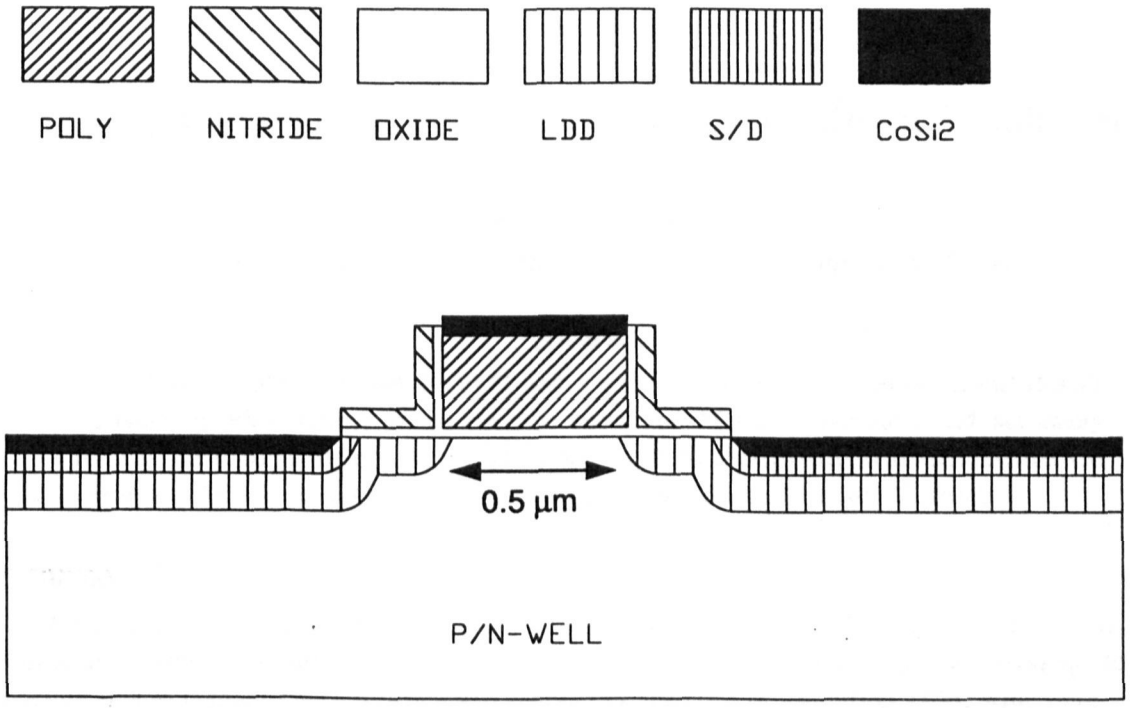

Figure 3. Cross section of a submicron LDD MOSFET.