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A Submicron MOSFET Model for Analog Circuit Simulation

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Abstract

A new MOSFET model for VLSI analog circuit simulation is presented. It includes all important physical effects which describe submicron MOSFET operation and accurately predicts drain and substrate currents. The model has been implemented in SPICE. Device and circuit simulation results show considerable improvements over present SPICE models.

1 Introduction

An accurate and computationally efficient model for submicron MOSFETs is crucial in the simulation of analog circuits. Many of the models used in circuit simulation are inadequate in modeling near-threshold characteristics and output conductance in saturation [1,2], which are very important factors in low voltage mixed analog-digital VLSI system design.

Models for analog circuit simulations must achieve good and continuous representation of current through the device over the complete range of modes of operation including saturation and weak, moderate and strong inversion. In addition the drain current and its derivatives must be continuous to avoid convergence problems and give proper description of the transconductance and output conductance which are of particular relevance in analog simulation.

The model presented here uses a semi-empirical formula for surface potential and an improved mobility model. It takes into account drift, diffusion and impact ionization currents and allows for accurate modeling of the moderate inversion and saturation regions of a submicron MOSFET. Additional effects included in the model are nonuniform doping, channel length modulation and drain/source parasitic resistances. The proposed SPICE compatible model properly describes submicron MOSFET operation in an efficient way and has been implemented in SPICE. Device and circuit simulation results show considerable improvements in accuracy over present SPICE models without sacrifice in computation time.

2 The Model

Consider a n-channel MOS transistor with the nonuniform doping profile modeled using box profile approximation as illustrated in Fig.1. The threshold voltage V_T is defined here as the gate-source voltage V_{GS} which corresponds to the onset of the moderate inversion [1] and is calculated for the given profile using the depletion approximation.

The surface potential in moderate and strong inversion is modeled using the following semi-empirical formula:

$$\phi_s = 2\phi_F - V_{BS} + n\frac{kT}{q}\frac{V_{GS}-V_T}{V_{GS}-V_T+V_0} \;;\; V_{GS}\geq V_T \qquad (1)$$

where n is a model constant which accounts for the changes of the surface potential as gate voltage

increases above the threshold and V_{BS} is the substrate voltage. The V_0 term in (1) was derived to ensure the continuity of the surface potential with respect to the gate voltage at $V_G = V_T$ and is given by:

$$V_0 = n\frac{kT}{q}\left[1 + \frac{\gamma}{2}\left[2\phi_F - V_{BS} - \frac{qDx_s}{2\varepsilon_s}\right]^{-0.5}\right] \tag{2}$$

where $\gamma = \sqrt{2\varepsilon_s qN_B}/C_{ox}$ is the body factor, C_{ox} is the gate oxide capacitance and $D = (N_S - N_B)x_s$ is the doping profile dependent parameter (see Fig.1). Equation (1) causes the surface potential to vary from $2\phi_F - V_{BS}$ at the threshold to $2\phi_F - V_{BS} + nkT/q$ at large gate voltages. A comparison between eq.(1) and numerical simulation is shown in Fig.2. As illustrated, the surface potential and its derivative are continuous and match the numerical results well. Using (1), the inversion layer charge at the source end of the channel Q_{inv} is expressed in moderate and strong inversion, using the concept of the effective threshold voltage V_T^*, by the following relations:

$$|Q_{inv}| = C_{ox}(V_G - V_T^*) \tag{3}$$

$$V_T^* = V_{FB} + \phi_s + V_{BS} + \frac{qD}{C_{ox}} + \gamma\left[\phi_s - \frac{qDx_s}{2\varepsilon_s}\right]^{0.5} \tag{4}$$

where V_{FB} is the flat-band voltage. The above relation for V_T^* includes the effect of nonuniform doping and the changes of the surface potential in moderate inversion. As shown in Fig.3, the accuracy of eq.(3), which directly impacts the accuracy of the drift current model, is very good as opposed to the standard linear approximation.

The drain current I_D is modeled as a sum of drift I_{drift}, diffusion I_{diff} and impact ionization I_{ion} components. Both drain and substrate currents and their derivatives are continuous in all regions of operation. The parasitic source and drain resistances are included in the model as external elements to preserve the model accuracy.

The carriers mobility is modeled using the standard relation for mobility degradation by the effective vertical field which in turn is expressed in terms of the inversion layer charge Q_{inv}, given by (3), and the depletion layer charge Q_B. The accuracy of the drift current model is directly affected by the velocity saturation model, particularly for deep-submicron devices. The "two-section" model [3] for the velocity saturation has been improved to predict the dependence of the drift velocity on the electric field more accurately, as shown in Fig.4. Using the gradual channel approximation the drift current in nonsaturation was derived to be:

$$I_{drift} = \beta_0\frac{\mu_{eff}}{\mu_0}(V_{GS} - V_T^* - \frac{a}{2}V_{DS})V_{DS} \tag{5}$$

where a and β_0 are given by:

$$a = 1 + \frac{\gamma}{2}\left[\phi_s - \frac{qDx_s}{2\varepsilon_s}\right]^{-0.5} \qquad \beta_0 = \frac{W}{L}\mu_0 C_{ox} \tag{6}$$

W and L are the effective channel width and length respectively, and μ_0 is the carriers zero-field mobility. The effective carriers mobility μ_{eff} is modeled by the following relation:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_G(V_{GS} - V_T^*) + \theta_B\left[\frac{qD}{C_{ox}} + \gamma(\phi_s - \frac{qDx_s}{2\varepsilon_s})^{0.5}\right] + \theta_D V_{DS}} \tag{7}$$

where θ_G, θ_B and θ_D are model parameters which describe mobility degradation due to gate-source, substrate-source and drain-source voltages.

To model the output conductance in saturation the concept of channel length modulation is used. The analytical expression for the channel length reduction ΔL is obtained by solving one-dimensional Poisson's equation in the high field region:

$$\Delta L = \frac{\left[E_C^2 + 2\left[a_s \frac{qN_S}{\varepsilon_s} + \frac{b_s}{C_{ox}} |Q_{inv}(L)|\right](V_{DS}-V_{DSAT})\right]^{0.5} - E_C}{a_s \frac{qN_S}{\varepsilon_s} + b_s \frac{|Q_{inv}(L)|}{C_{ox}}} \tag{8}$$

where a_s and b_s are two empirical model parameter which control output conductance in the low and high current region respectively. E_C is the critical field for carriers saturation. The inversion layer charge at the drain end of the channel $Q_{inv}(L)$ is modeled in a similar manner as $Q_{inv}(0)$ given by (3). An expression for the saturation voltage V_{DSAT} is derived using carriers velocity saturation model, which completes the formulation of the drift current model.

The diffusion current I_{diff} is modeled using Barron's expression [4] modified to model the saturation of the diffusion current as V_{GS} voltage increases above the threshold:

$$I_{diff} = \beta_0 \gamma k_s \left(\frac{kT}{q}\right)^2 \frac{\exp\left[\frac{\phi_s - 2\phi_F + V_{BS}}{kT/q}\right]}{1 + s\exp\left[\frac{\phi_s - 2\phi_F + V_{BS}}{kT/q}\right]} \left[1 - \exp\left(-\frac{V_{DS}}{kT/q}\right)\right] \tag{9}$$

where k_s model parameter controls the subthreshold slope and s controls the degree of saturation of the diffusion current. This modified relation is used to model diffusion current in all regions of operation, as shown in Fig.5, not only in weak inversion as original expression proposed in [4]. The contribution of both drift and diffusion currents to the total current is illustrated in Fig.6. As shown, in the moderate inversion the contribution of both components of the current is important. Therefore, the accuracy of moderate inversion modeling is greatly improved here by avoiding artificial separation of the drain current equations into weak and strong inversion regions as it has been done in standard SPICE models.

The last component of the drain current, the impact ionization current I_{ion}, is modeled using the expression proposed in [5]:

$$\frac{I_{ion}}{I_D} = A_i(V_{DS}-V_{DSAT}) \exp\left[-\frac{B_i}{(V_{DS}-V_{DSAT})}\right] \tag{10}$$

where A_i and B_i are process dependent model parameters. The saturation voltage V_{DSAT} needs to be very accurately modeled since the I_{ion} current depends exponentially on the $V_{DS}-V_{DSAT}$ difference. The relation for the saturation voltage V_{DSAT}, based on the improved model of velocity saturation, is more accurate than standard models and therefore the substrate current and output conductance degradation caused by hot electrons are modeled more accurately.

3 Results

The model predictions were compared to experimental results on MOSFET devices fabricated using a n+ polysilicon gate submicron CMOS process. Both p-channel (buried-channel) and n-channel (surface-channel) devices with different geometries were measured.

Model parameters were extracted using optimization techniques. Drain and substrate currents as well as transconductance and output conductance errors were minimized simultaneously, a necessary step for analog circuit simulation. To obtain values that are physically meaningful a hierarchical parameter extraction scheme was used. This involved identifying device operating regions such that only a selected set of model parameters are dominant in each region. The novel identification scheme based on the current levels and voltages was used which ensures physical meaning of the extracted model parameters and also reduces the number of iterations in the optimization loop.

Typical experimental results are shown in Figs. 7-11. As illustrated drain current as well as transconductance and output conductance are modeled very accurately. As an additional test for the model, the saturation voltage was measured independently on devices with different channel lengths using the technique proposed in [5]. As illustrated in Fig.12 the match between the model and experimental results is excellent.

In general, the new model is more accurate than standard SPICE models (levels 2 and 3). Some other models such as BSIM [6] and CSIM [7] were also used for comparison, but their predictions were no better than for standard SPICE models. The increase in accuracy of transconductance and output conductance modeling resulting from using the new model is typically more than a factor of two with respect to standard SPICE models.

The new model was implemented in the SPICE 3 circuit simulator. A folded cascode CMOS operational amplifier, shown in Fig. 13, was simulated to compare accuracy and execution time using different models. The ac low frequency open-loop gain of the amplifier was calculated using the new model to be 42dB, close to the measured value of 40dB. However, using the SPICE level 3 model, the open-loop gain was calculated to be 47dB (200% error as compared to experiment). The significant increase in the simulation accuracy using the new model is mainly due to reduced errors in the transconductance and the output conductance in moderate inversion where most of the devices in the signal path are operating.

4 Conclusions

A new MOSFET model valid in all regions of operation has been developed, verified experimentally and implemented in the SPICE 3 circuit simulator. It is physically based, accurate and suitable for both analog and digital applications. These properties make the model very useful in the development of future mixed analog-digital VLSI systems.

Acknowledgments

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References

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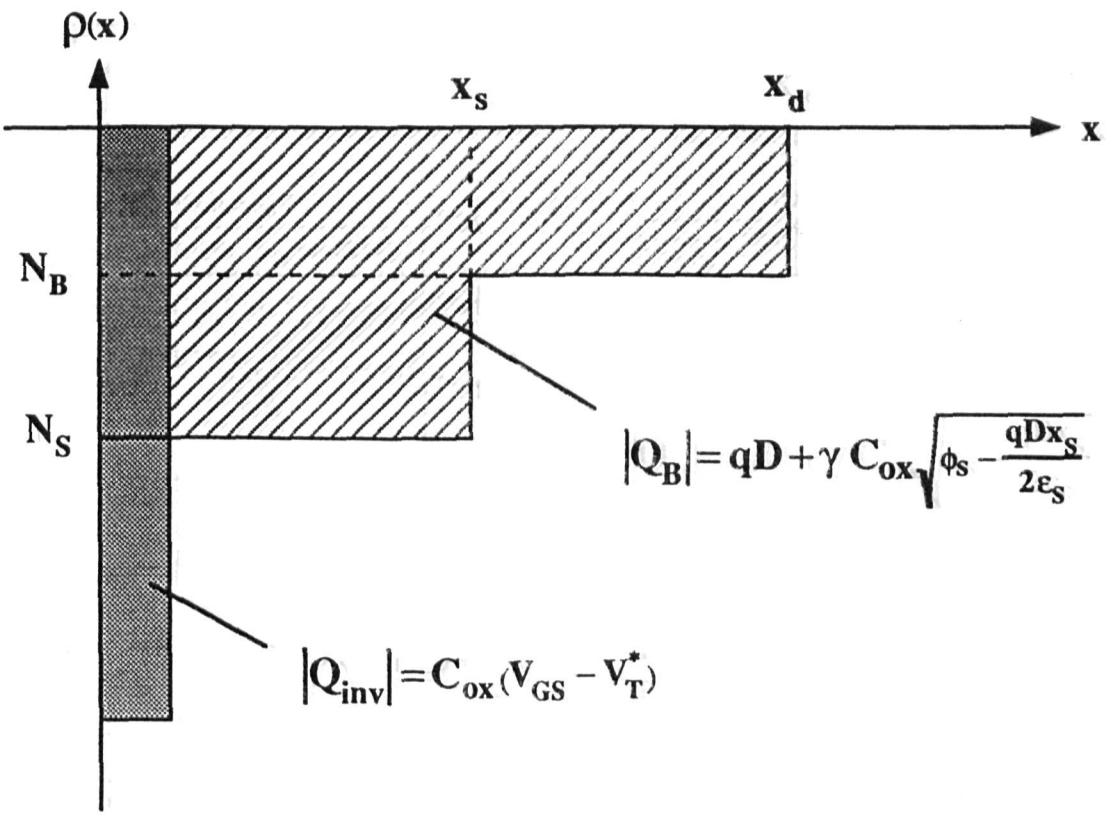

Fig. 1 Charge density $\rho(x)$ in a n-channel MOSFET with a box doping profile. x_d is the depletion layer width and x_s is the width of nonuniformly doped region.

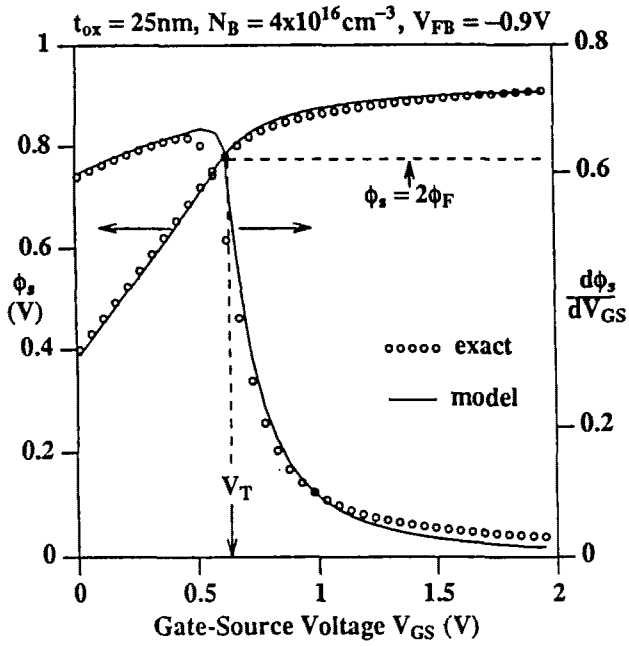

Fig.2 Surface potential ϕ_s vs. V_{GS} voltage.

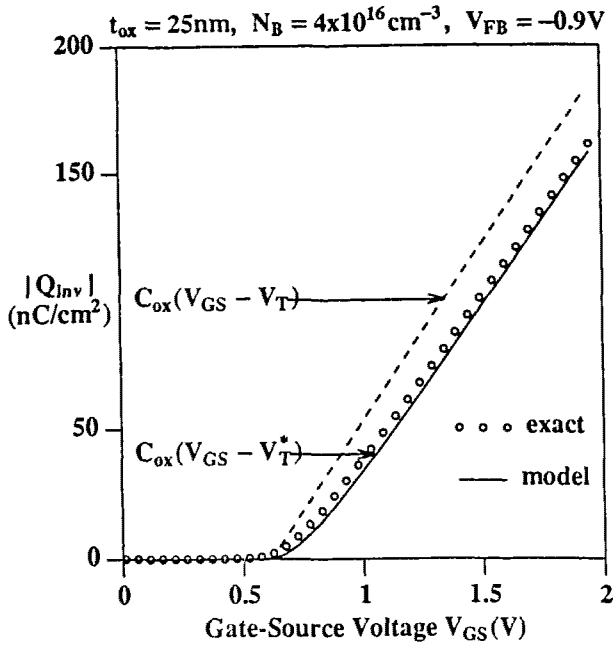

Fig.3 Inversion layer charge Q_{inv} vs. V_{GS}.

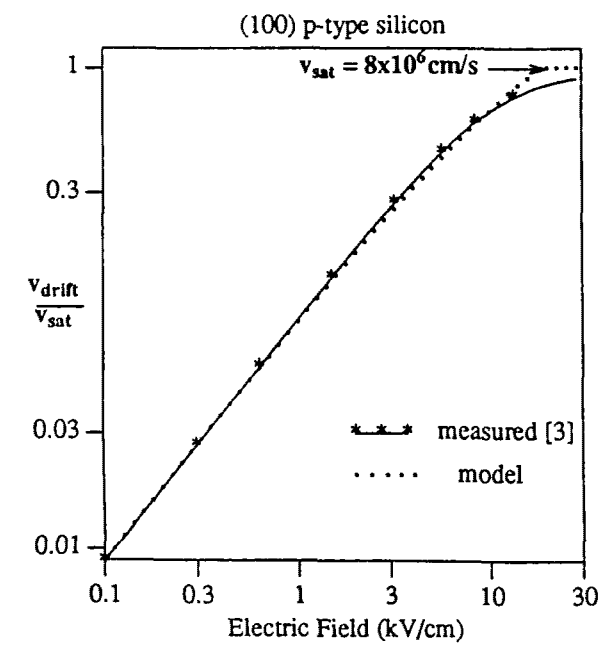

Fig.4 Electron drift velocity vs. electric field.

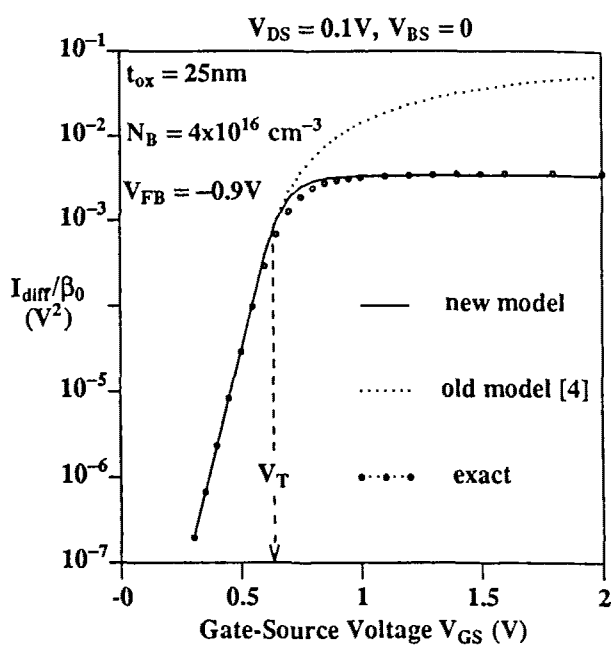

Fig.5. Normalized diffusion current I_{diff} vs. V_{GS}.

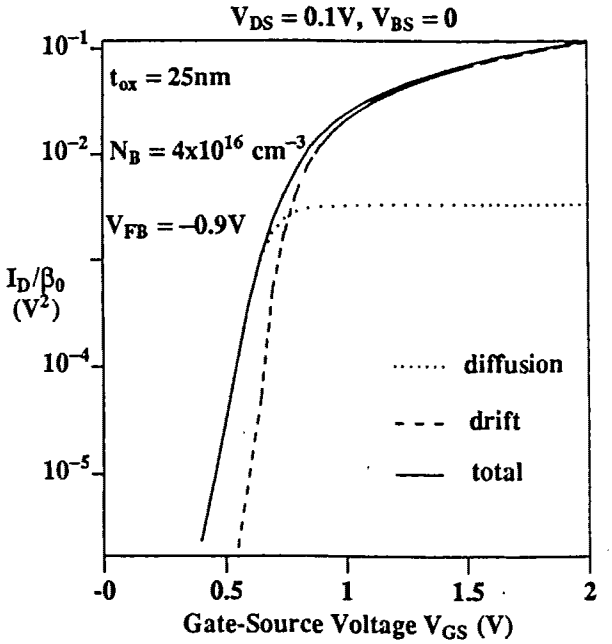

Fig.6 Drain current and its components vs. V_{GS}.

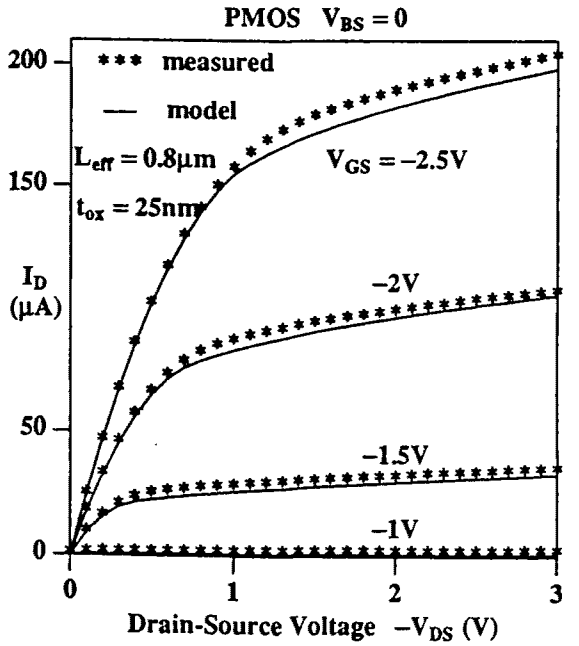

Fig.7 Output characteristics I_D vs. V_{DS}.

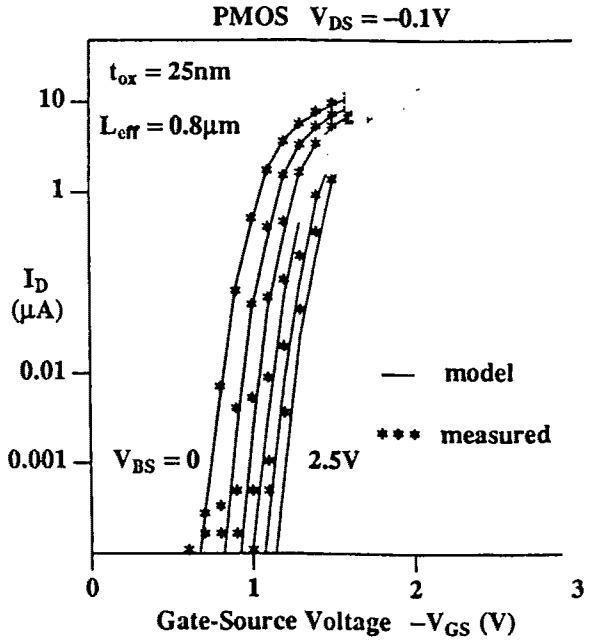

Fig.8 Subthreshold characteristics I_D vs. V_{GS}.

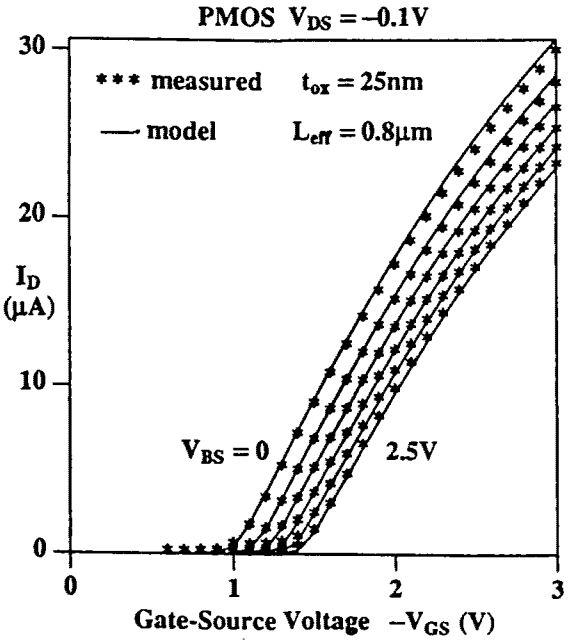

Fig.9 Transfer characteristics I_D vs. V_{GS} voltage.

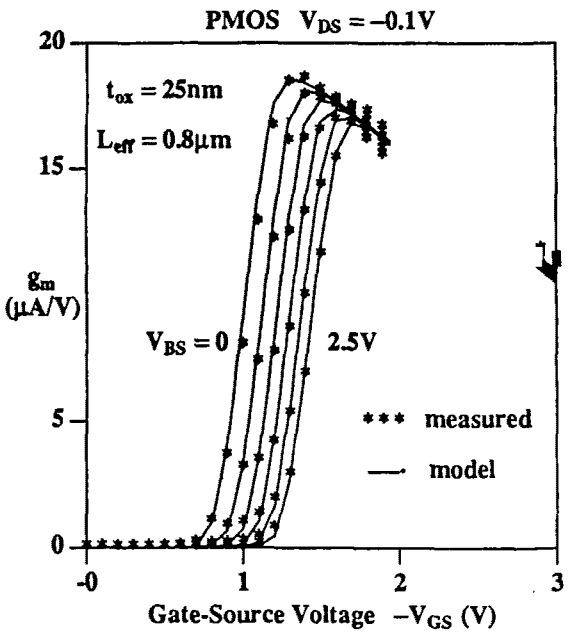

Fig.10 Transconductance g_m vs. V_{GS} voltage.

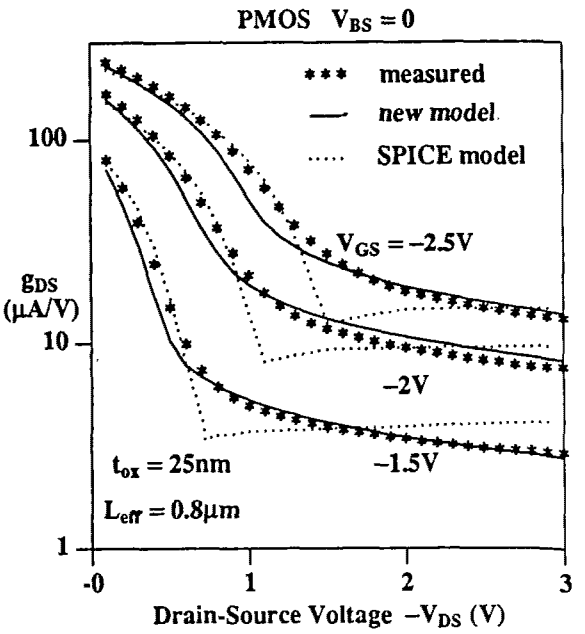

Fig.11 Output conductance g_{DS} vs. V_{DS} voltage.

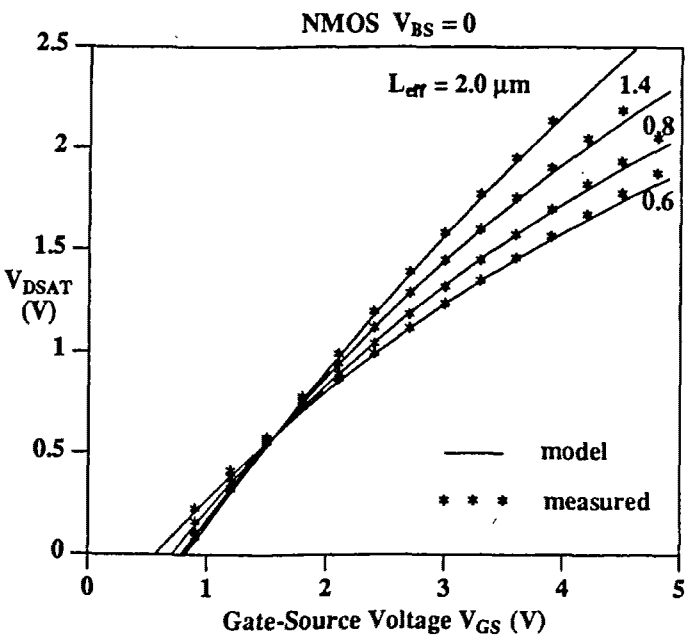

Fig.12 Saturation voltage V_{DSAT} dependence on V_{GS}.

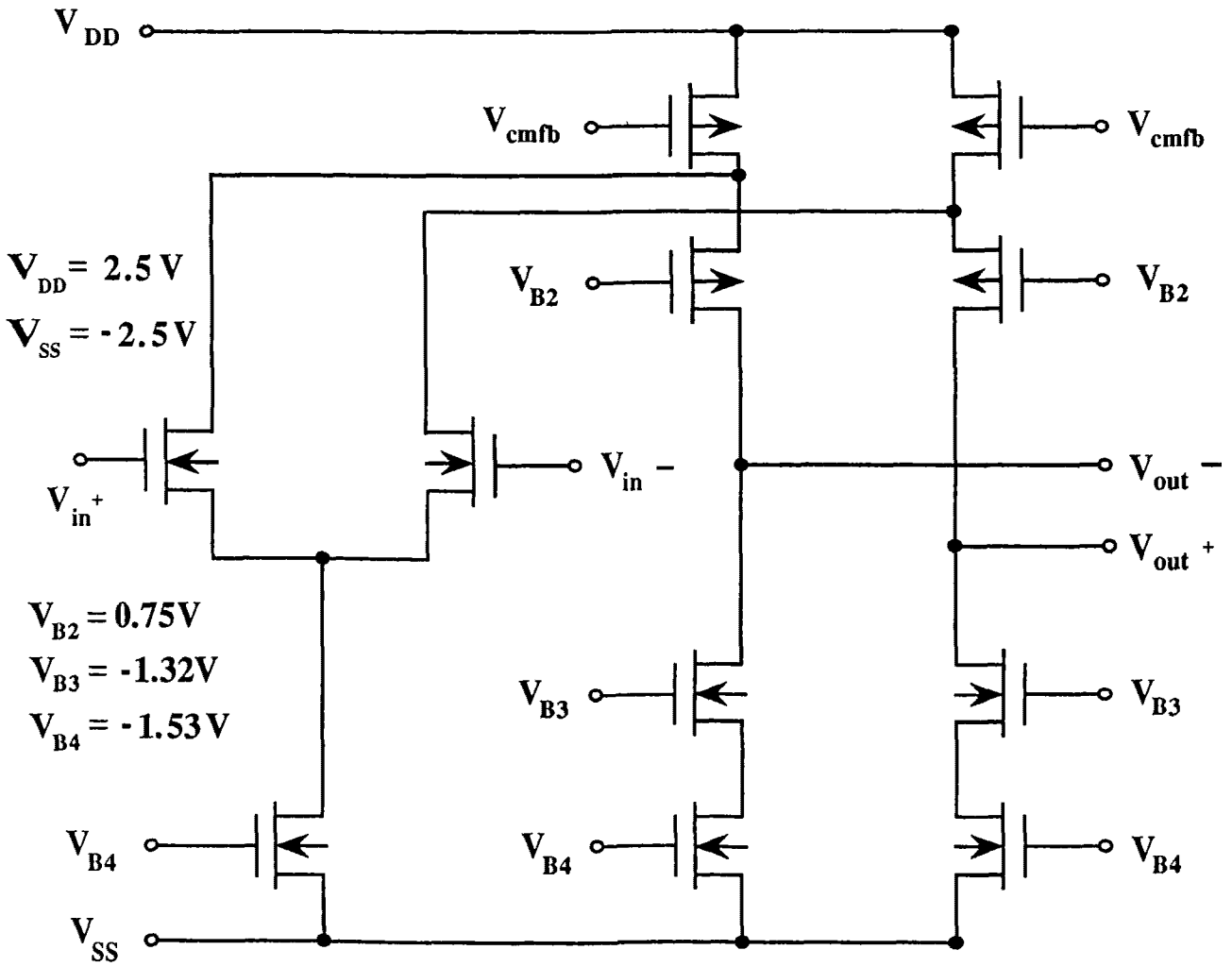

Fig. 13 Schematic diagram of the cascode gain section and input stage of the differential folded-cascode amplifier. V_{cmfb} represents the common-mode feedback signal.