SIMULATION OF SEMICONDUCTOR DEVICES AND PROCESSES Vol. 3
Edited by G. Baccarani, M. Rudan - Bologna (Italy) September 26-28, 1988 - Tecnoprint

Bipolar Circuit Simulation System using a Two-Dimensional Device Simulator

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Abstract

To accurately estimate the performance of bipolar circuits, two circuit simulation systems using a two-dimensional device simulator have been developed and compared. One system uses the table method, and the other uses the direct method. Simulations of an ECL gate inverter chain, and propagation delay simulations of the two methods were compared.

1. Introduction

Device simulator can simulate device behaviors exactly because it can reflect the device structure exactly and also can simulate physical phenomena accurately. Usually only device characteristics are examined and the circuit performance is estimated from these characteristics. As a result, a simulation system that estimate circuit performance using the two-dimensional device simulator is strongly desired.

One example of this type simulator is MEDUSA[1]. In MEDUSA, only a one-dimensional device simulator of bipolar devices is installed. Therefore, we developed two types of circuit simulators using two-dimensinal device simulators. One uses numerical tables to contain the transistor equivalent circuit element information. These tables are made from the stationary solutions of the device simulator. The other type of circuit simulator solves circuit equations directly by using the transient solutions of the device simulator. We call the former the

"table method", and the latter the "direct method."
In this paper, we present and compare the simulation techniques of these two methods.

2. Simulation Method

Figure 1 depicts the simulation flow for circuit performance. The analytical model in a conventional circuit simulator has many parameters which are extracted from the device simulator results. This is shown by the arrows labelled 1. However, this parameter extraction is often a very elaborate task, and dominant factors essential for high speed operation, for example, high current injection, diffusion capacitance, and two-dimensional effects, cannot be described exactly by the analytical transistor model.

The table method uses numerical tables from the two-dimensional device simulator without extracting model parameters. This is shown by arrows labelled 2.

The direct method does not use the equivalent circuit, but solves the nodal equations using transient solutions of the device simulator. This is shown by arrows labelled 3.

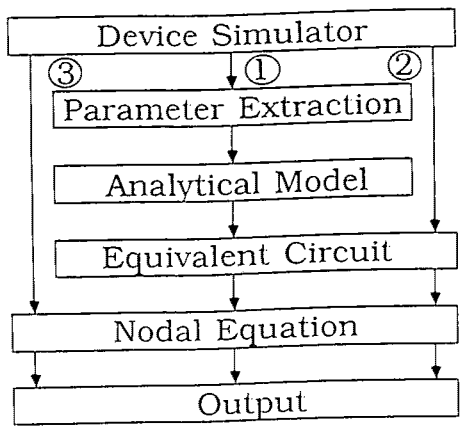


Fig. 1 Simulation flow to get circuit performance.

2.1 Device Simulator

Device simulator FLAPS(Fujitsu Laboratories Analysis Program of Semiconductor devices) solves the following basic semiconductor equations.

$$\mathrm{div}(\varepsilon \mathrm{grad}\psi) = -q(p - n + N_D - N_A). \quad (1)$$

$$dn/dt = 1/q\ \mathrm{div}J_n + G - R. \quad (2)$$

$$dp/dt = -1/q\ \mathrm{div}J_p + G - R. \quad (3)$$

$$J_n = -qn\mu_n \mathrm{grad}\phi_n. \quad (4)$$

$$J_p = -qp\mu_p \mathrm{grad}\phi_p. \quad (5)$$

$$n = n_{ie}\ \exp\{q/kT(\psi - \phi_n)\}. \quad (6)$$

$$p = n_{ie}\ \exp\{q/kT(\phi_p - \psi)\}. \quad (7)$$

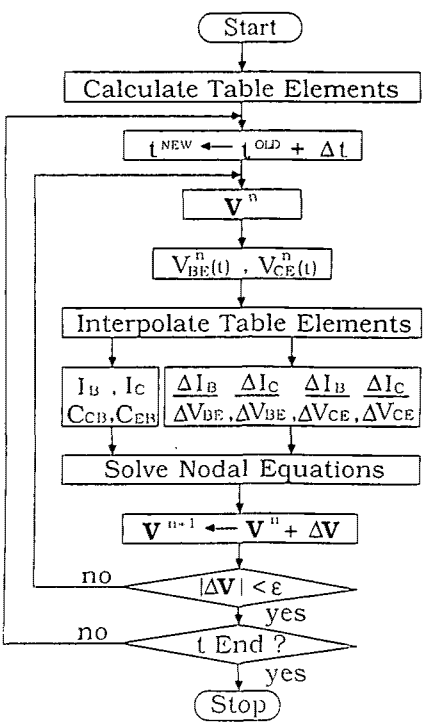


Fig. 2 Simulation flow of the table method.

Here, G is a generation rate term, and R is a recombination rate term, and ϕ_n and ϕ_p are quasi-Fermi potentials of an electron and a hole respectively, and n_{ie} is an intrinsic carrier density. These equations are discretized by a finite difference method and are solved using the incomplete LU decomposition conjugate gradient method[3]. This program is also vectorized for a vector processor.

2.2 Table Method

Figure 2 depicts the simulation flow for the table method. Before solving nodal equations, we must develop numerical tables for the equivalent circuit elements. In this method, we adopted the equivalent circuit shown in Fig. 3. Capacitances and current sources in this equivalent circuit are obtained from the two-dimensional device simulator solutions.

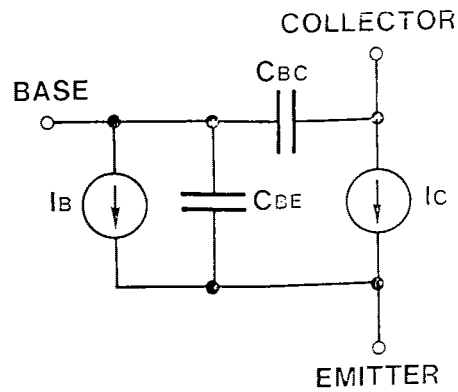


Fig. 3 Equivalnet circuit of a bipolar transistor used in the table method.

The current tables are obtained from the terminal currents of the base and the collector. To make the capacitance tables, the total charge Q in the device was obtained from the following relation.

$$Q=\int \rho ds. \qquad (8)$$

From the derivatives of the total charge with respect to the terminal voltages, two capacitances are obtained:

$$C_{EB}=\Delta Q/\Delta V_{EB} \cdot \quad (9)$$

$$C_{CB}=\Delta Q/\Delta V_{CB} \cdot \quad (10)$$

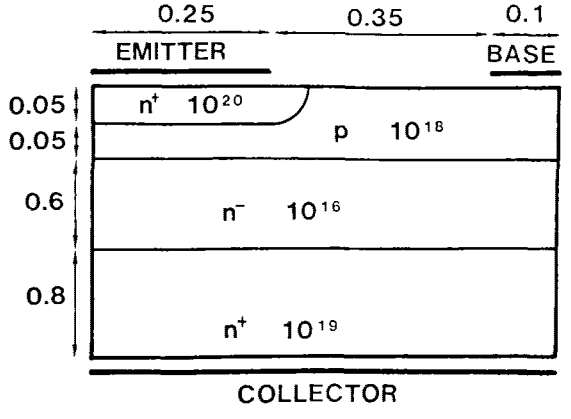
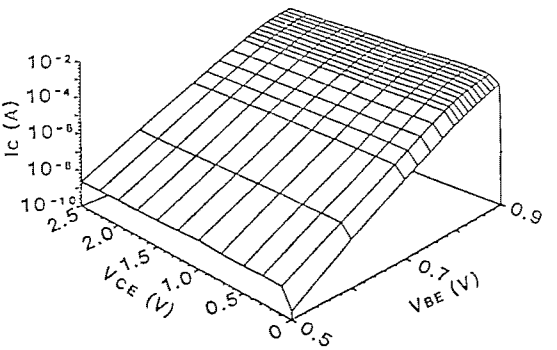


Fig. 4 Simulation structure of a bipolar transistor.

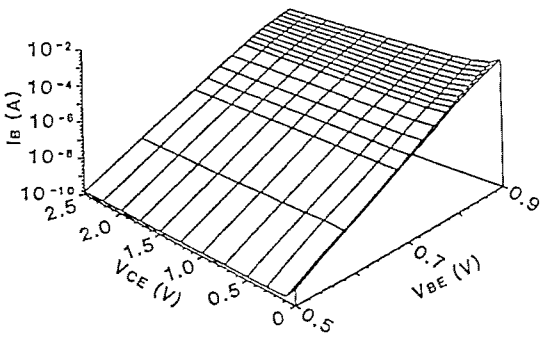
Figure 4 is a diagram of the simulated structure of a bipolar transistor. Considering symmetry, only half of the device needs be simulated. This structure has an emitter width of 0.05 μm and a base width of 0.05 μm.

Figure 5 illustrates the two-dimensional numerical tables of currents and capacitances. Dividing maximum collector-emitter voltage of 2.5 V into 12 elements and also maximum base-emitter voltage of 0.9 V into 17 elements, two-dimensional numerical tables of the base current I_E and the collector current I_C were obtained. The 17x7 element capacitance tables were made in the same way. Irregular spaced elements were adopted for increased accuracy in the high current region. Values of inter-element points are obtained by linear interpolations of the logarithmic values. By a vectorized program, it took 33 minutes of CPU time for a Fujitsu VP100 vector processor to make these numerical tables.

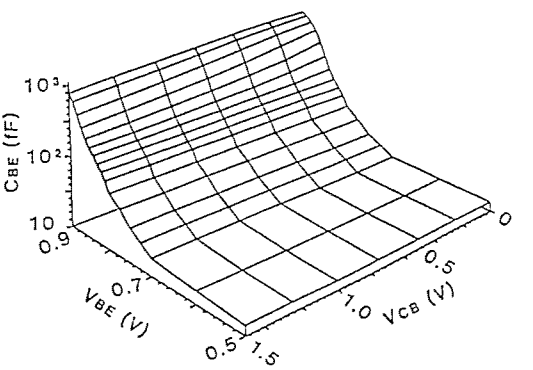
Extrinsic components, like an extrinsic poly Si base resistance and a collector-substrate capacitance, are attached externally to the equivalent circuit of Fig. 3.



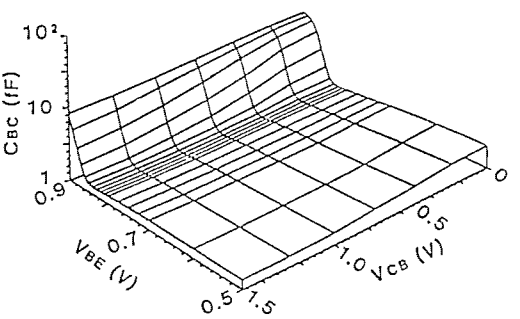
(a)
$I_C(V_{CE},V_{BE})$



(b)
$I_B(V_{CE},V_{BE})$



(c)
$C_{BE}(V_{BE},V_{CB})$



(d)
$C_{BC}(V_{BE},V_{CB})$

Fig. 5 Numerical tables of the table method.

Generally, the nodal equations are expressed as follows.

$$\sum_{j} I_{ij}=0 \quad (i=1,N). \tag{11}$$

Here, N is a total node number and I_{ij} is a current which flows into the i-th node. These equations are discretized with respect to time. Discretized time intervals are between 0.2 ps and 5 ps. We solved these equations by Newton's method at each time interval.

In the Newton's method, non-linear currents of a bipolar transistor are linearized as follows.

$$I_B=I_{B0}+\frac{\partial I_B}{\partial V_{BE}}\Delta V_{BE}+\frac{\partial I_B}{\partial V_{CE}}\Delta V_{CE}. \tag{12}$$

$$I_C=I_{C0}+\frac{\partial I_C}{\partial V_{BE}}\Delta V_{BE}+\frac{\partial I_C}{\partial V_{CE}}\Delta V_{CE}. \tag{13}$$

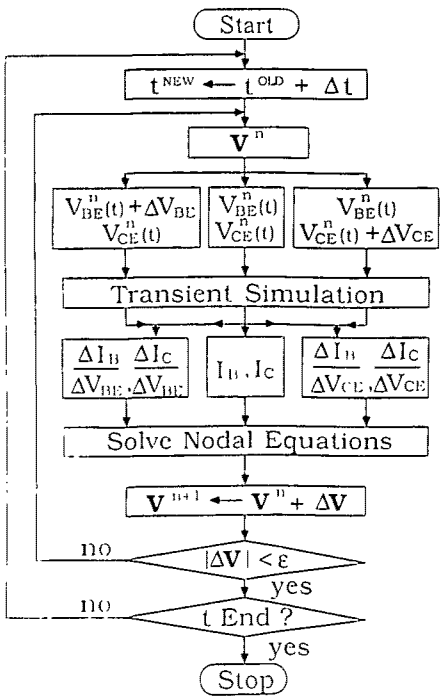


Fig. 6 Simulation flow of the direct method.

In these equations, derivatives of the currents with respect to the voltages are obtained from the numerical tables by linear interpolation of logarithmic values.

2.3 Direct Method

Circuit behavior is essentially a transient phenomenon. Therefore, the use of transient solutions is the best to simulate the circuit behavior. Figure 6 shows the simulation flow for the direct method. Currents and current derivatives are obtained from the transient solutions of the two-dimensional device simulator, and are used to solve the nodal equations.

First, the basic semiconductor equations (1)-(7) are solved transiently for three terminal voltages for each transistor by increasing the time by Δt. The base and the collector currents are then obtained. The bias conditions for transient anaysis are shown in Table 1.

Terminal Voltage		Terminal Current	
Base	Collector	Base	Collector
$V_{BE}(t)$	$V_{CE}(t)$	I_{B1}	I_{C1}
$V_{BE}(t)+\Delta V_{BE}$	$V_{CE}(t)$	I_{B2}	I_{C2}
$V_{BE}(t)$	$V_{CE}(t)+\Delta V_{CE}$	I_{B3}	I_{C3}

Table 1. Bias condition for transient simulations.

Using these currents, the derivatives of the currents with respect to the terminal voltages are as follows.

$$\frac{\partial I_B}{\partial V_{BE}} = \frac{I_{B2}-I_{B1}}{\Delta V_{BE}} \quad . \tag{14}$$

$$\frac{\partial I_B}{\partial V_{CE}} = \frac{I_{B2}-I_{B1}}{\Delta V_{CE}} \quad . \tag{15}$$

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{I_{C2}-I_{C1}}{\Delta V_{BE}} \quad . \tag{16}$$

$$\frac{\partial I_C}{\partial V_{CE}} = \frac{I_{C2}-I_{C1}}{\Delta V_{CE}} \quad . \tag{17}$$

Here, ΔV_{BE} is 0.01 V and ΔV_{CE} is 0.05 V. These calculations are performed for each transistor. The nodal equations are solved using these current and current derivatives. This procedure is repeated until the solutions of the nodal equations converge. When nodal equations converge, time is increased by Δt, and the calculations are repeated.

In the table method, or the quasi-static approach, nodal equations are solved using the stationary solutions. However, in the direct method, or non-quasi-static approach, the nodal equations are solved using the transient solutions. The direct method is thus considered to be superior to the table model because the quasi-static approach is not used and purely transient phenomena can be evaluated.

2.4 Determination of Circuit Elements

To compare circuit speeds, the logic swing of an ECL gate is kept constant. In these simulation systems resistances in an ECL gate can be automatically determined by DC solutions of the table method when the transistor size is given.

3. Comparison

Assuming that exact solutions are obtained by the direct method, we examined the accuracy of the table method. Difference between propagation delays of an ECL gate was investigated. Propagation delays were obtained from the simulation of the three-stage inverter chain shown in Fig. 7. The ECL gate has an emitter follower and supply voltage of -3.1 V, an emitter follower supply voltage of -1.8 V, and a reference voltage of -1.2 V.

Figure 8 graphs the output waveforms, simulated with the direct method, of this inverter chain when a step voltage with a 50 ps fall time was applied to the input terminal. The propagation delay per gate was obtained from the time difference between the output voltages of the first and the third stages. In this case, the propagation delay per gate was 57 ps and the consumed power per gate was 3.08 mW. It took 3.7 hours of CPU time for a Fujitsu VP100 vector processor to obtain this result. Figure 9 plots consumed power dependence of the propagation delay for the two methods.

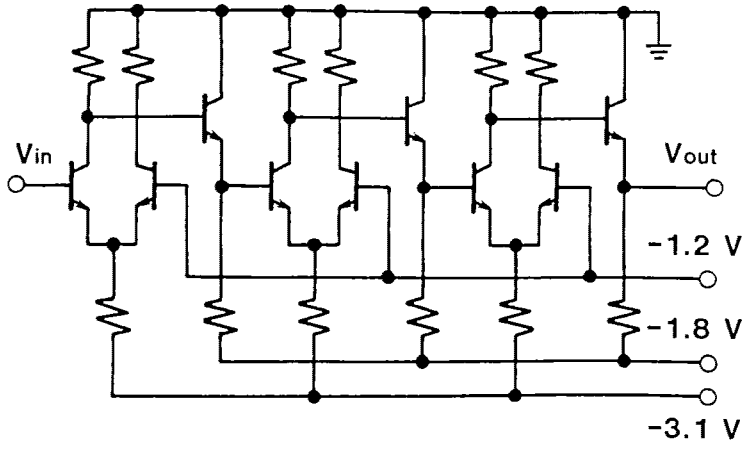


Fig. 7 Three-stage ECL gate inverter chain.

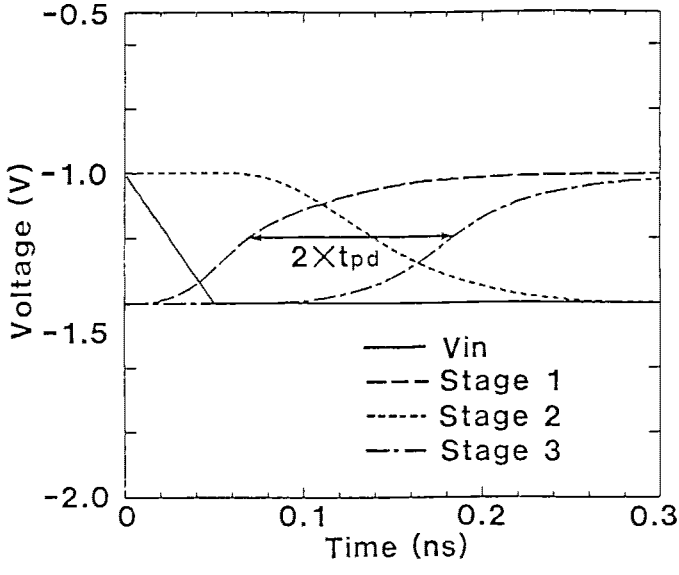


Fig. 8 Output waveforms of an inverter chain.

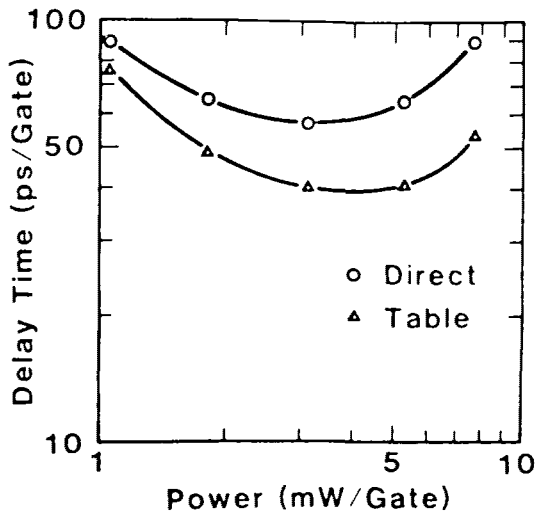


Fig. 9 Comparison of propagation delay for the tabel method and the direct method.

The table model gives smaller propagation delay than the direct method in the whole power region. The difference between the two methods is larger in the high power region than in the low power region. The reason is that, in the table method, the time delay in the extrinsic base region cannot be exactly estimated, and because influence of the extrinsic base resistance is already included in the current tables, and also because extrinsic base-collector capacitance is also included in the capacitance C_{BC}.

Therefore, in the table method, the propagation delay discrepancy increases when it is determined by the time delay of extrinsic transistor elements.

4. Summary

We developed two simulation systems which estimate the performance of bipolar circuits using a two-dimensional device simulator.

The table model using stationary solutions gives exact solutions for DC analysis. However, for transient analysis. it gives inaccurate results especially in the high power region because of both the incorrect equivalent circuit and the quasi-static approach.

The direct method is considered to be the most accurate method to simulate circuit behaviors, but needs much CPU time.

As a near future problem, both improvements of CPU time in the direct method and of the equivalent circuit of the table model must be done.

Acknowledgement

The authors wish to thank Mr. H. Ishikawa for encouragement and thank Mr. M. Kokado and Prof. W. L. Engl for their fruitful discussions and also thank Dr. K. Hane for useful advice for development of device simulator.

References

[1] W.L.Engl, R.Laur, and H.K.Dirks, "MEDUSA-A Simulator for Modular Circuits", IEEE Trans. Computer-Aided Des., Vol. CAD-1, pp85-93, 1982.
[2] L.W.Nagel, "SPICE 2-A Computer Program to Simulate Semiconductor Circuits", University California, Berkeley, ERL Memo ERL-M520 (1975-5)
[3] G.Abe, K.Hane, and T.Suzuki, "Device Simulation Code for Vector Processor", Proceedings of NASECODE IV, pp123-128, 1985