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AVALANCHE BREAKDOWN IN THE ALDMOST

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SUMMARY

Recently a new lateral power MOSFET structure named accumulation lateral DMOS transistor (ALDMOST) has been proposed. We have investigated the dependence of high voltage breakdown caused by impact ionization on the oxide thickness and the additional semi-insulating layer along the surface of the gate oxide above the drift region. The simulations have shown that the breakdown voltage will not be lowered in a critical way compared to the conventional LDMOST.

INTRODUCTION

The recently proposed power MOSFET named accumulation lateral DMOS transistor (ALDMOST) is a modified LDMOS structure with an additional semi-insulating layer along the surface of the gate oxide above the drift region (Habib, 1987). This layer has been introduced in order to lower the high ON-resistance of the device (Nanz, 1988a), which is in general a disadvantage of this type of MOS transistors. These devices are used as output driver devices for high voltage CMOS structures therefore the breakdown behaviour is of particular importance.

In our computations with the two-dimensional device simulation program BAMBI we have compared the ALDMOST with a conventional LDMOST which has been investigated previously (Nanz, 1987).

PRINCIPLE OF OPERATION

In Fig. 1 the geometry of the transistor can be seen, which we have investigated. It is an n-channel device with a semiconductor area of $82\mu m \cdot 49\mu m$ and a channel length of approximately $2\mu m$. In Fig. 1 the voltage distribution between the gate and the drain contact along

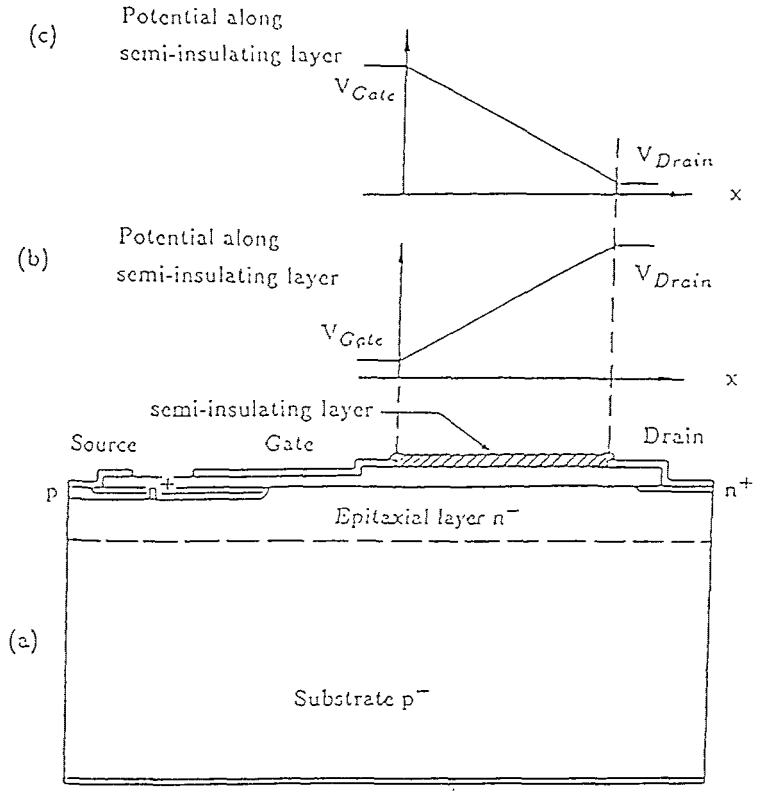

Fig. 1 Geometry and voltage distribution along semi-insulating layer
(a) Geometry
(b) Voltage distribution in OFF-condition
(c) Voltage distribution in ON-condition

the semi-insulating layer is also given. This varying voltage (in space) is enabled by an semi-insulating polycristalline silicon (SIPOS) layer which is provided on the surface of the oxide above the drift region. The SIPOS layer is connected at both ends to the gate and drain contacts, respectively, in order to guarantee a uniform potential distribution (Mukherjee, 1986). In OFF-condition the surface electric fields in the semiconductor are significantly reduced, in ON-condition the ON- resistance is lowered up to a factor of 3 depending on the oxide thickness.

For our simulations we have varied the oxide thickness between 0.4 μm and 0.1 μm. The doping profile is approximated by Gaussian distribution functions. The maximum values are shown in Table 1.

Table 1. Maximum values of doping profile

n^+ [cm^{-3}]	p [cm^{-3}]	n^- [cm^{-3}]	p^- [cm^{-3}]
$2.0 \cdot 10^{20}$	$5.0 \cdot 10^{16}$	$3.0 \cdot 10^{14}$	$1.2 \cdot 10^{14}$

AVALANCHE BREAKDOWN

Avalanche breakdown occurs in regions with large peaks in the electric field either from the drain contact through the substrate or at the p-n-junction from the channel to the drift region. In our device the latter effect can be observed. These peaks in the electric field are reduced by the additional semi-insulating layer in the ALDMOST because of the uniform voltage distribution at top of the oxide. Furthermore a larger amount of drift region charge can be provided, because the bias of the semi-insulating layer enhances the depletion of the drift region from the surface (Mukherjee, 1986). Therefore a breakdown voltage at least as high as for the LDMOST might be expected.

On the other hand the breakdown voltage will be reduced by the additional bias since the effective distance between the drain and the gate contacts is decreased by the electron accumulation in the drift region near the drain contact (Colak, 1980). This means that the effective length of the drift region is reduced.

To get a more complete understanding of the qualitative and quantitative behaviour of the device near breakdown we have performed a simulation of all relevant features.

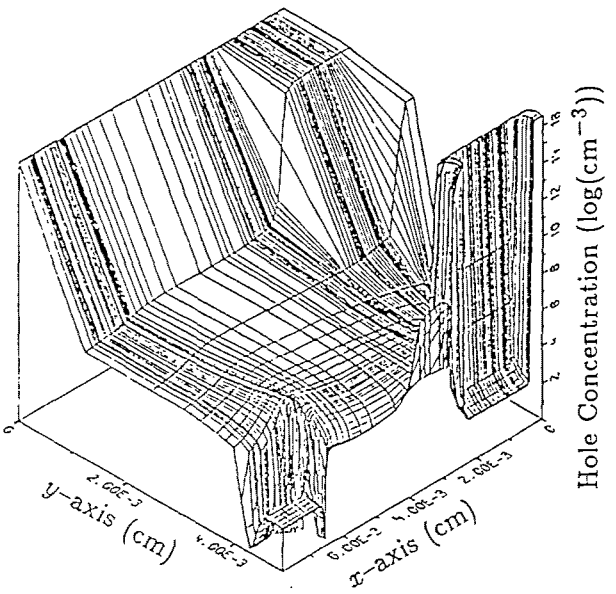

Fig. 2 Hole concentration at 440V for LDMOST

NUMERICAL METHODS

The computations have been carried out with our fully two-dimensional device simulator BAMBI which solves the three basic semiconductor equations simultaneously in a totally selfconsistent way utilizing a fully self-adaptive Finite Boxes grid (Franz, 1985; Nanz, 1988b). It should be pointed out that the effects of impact ionization are completely taken into account according to the avalanche model by van Overstraeten (1970). From our experience simple estimates with an ionization integral are not sufficiently accurate, since in particular the holes generated by impact ionization influence not only quantitatively but also qualitatively the space charge distribution.

For our simulations we have handled the SIPOS layer as a contact at the oxide above the drift region with a linearly varying potential (in space). The reduction of the peaks in the electric field could also be observed in the self-adaptive grid of our program: In the solutions of the semiconductor equations a singularity in the electric field arises at the change of the boundary conditions on a planar boundary. This singularity strongly influences the automatic grid refinement since for an estimation of the computational error the local truncation error of the Poisson equation is utilized. From the mathematical point of view the boundary condition of the ALDMOST along the gate contact, the SIPOS layer and the drain is a steady function, at both ends of the free surface of the LDMOST there is a change of the boundary conditions.

This effect could also be observed in the final number of grid points which was necessary to gain the same accuracy of the solution: about 10% less for the ALDMOST compared with the LDMOST.

One more point of interest should be mentioned. Computations accounting for all effects of impact ionization need a special treatment for the self-adaptive grid control. Since the change in the net generation/recombination R (right side of continuity equations for electrons and holes: $\mathrm{div}\ \vec{J}_n - q \cdot \frac{\partial n}{\partial t} = q \cdot R$, $\mathrm{div}\ \vec{J}_p + q \cdot \frac{\partial p}{\partial t} = -q \cdot R$) is of order 10^{30} cm^{-3} s^{-1} over the whole device, simple scaling of the values cannot provide sufficiently accurate results. Therefore we have implemented an additional criterion for automatic grid control: It has turned out that in areas with $|R| > 10^{22}$ cm^{-3} s^{-1} new points have to be inserted because otherwise not all physical effects in the device can be observed. As minimum grid distance the mean free path of electrons in the device material (about $60 \cdot 10^{-8}$cm for silicon) should be taken (Nanz, 1988b). The value of 10^{22} has been established by various numerical experiments.

It should be pointed out that by this strategy the convergence behaviour and speed of the iterative Newton cycle could significantly be improved. Nevertheless the complete breakdown simulation of one device geometry took about 20 CPU-hours on a VAX 8800.

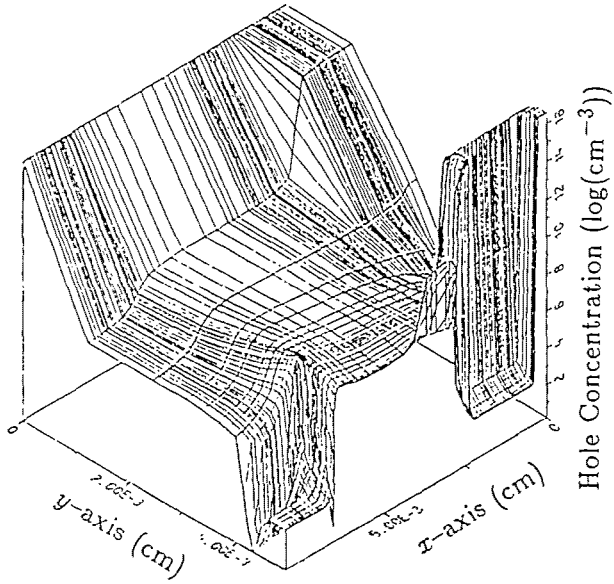

Fig. 3 Hole concentration at 470V for LDMOST

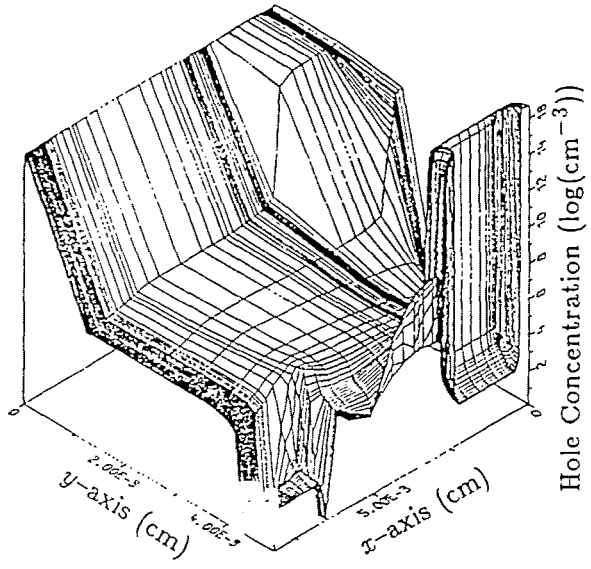

Fig. 4 Hole concentration at 470V for ALDMOST

NUMERICAL RESULTS

From our simulations almost the same breakdown voltages for both devices have been obtained. It is about 470V nearly independent of the oxide thickness. The difference between the values for both devices is less than 5%. In Fig. 2 and Fig. 3 the hole distributions for the

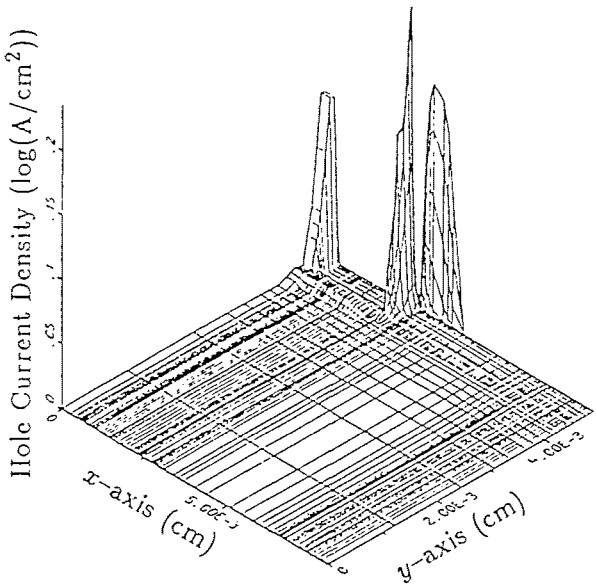

Fig. 5 Hole current density at 480V for LDMOST

LDMOST at 440V and 470V, repectively are shown. It can nicely be observed how the hole concentration raises over the whole device, especially in the channel region. This means that the breakdown will occur by avalanching at the p-n junction to the drift region. In Fig. 5 the hole current density of the LDMOST at the breakdown is shown for an applied voltage of 480V. There is significant hole current flow from the drift region through the channel towards the source contact.

From Fig. 3 and Fig. 4 an obvious tendency of the ALDMOST becomes clear to provide a lower voltage stability than the LDMOST because the high hole concentration induced by impact ionization at the interface between the oxide under the semi-insulating layer and the semiconductor area leaks far into the drift region. This particularly holds true for an oxide thickness larger than about 0.2μm. During our simulations it has been observed that this loss of voltage stability will be lowered if the oxide thickness is decreased. This means that the ALDMOST with an oxide thickness less than 0.1μm as described by Habib (1987) will exhibit almost the same breakdown voltage as the conventional LDMOST.

CONCLUSION

The breakdown voltage of the accumulation lateral DMOS transistor will slightly be decreased by the additional semi-insulating layer compared to the LDMOST but according to our results not in a critical way. The lower ON-resistance of the ALDMOST is therefore a real advantage compared to the conventional LDMOST. Furthermore we have presented a new criterion for automatic grid control in high voltage computations accounting for the influence of impact ionization.

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