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ELECTRICAL PERFORMANCES EVALUATION OF ISOLATION STRUCTURES BY COUPLED PROCESS AND DEVICE SIMULATIONS.

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ABSTRACT

Two-dimensional coupled process/device simulations have been used to characterize isolation properties of semi-recessed and fully-recessed LOCOS structures. The simulation results in excellent agreement with measurements demonstrate the sensitivity of the studied devices to the Si/SiO_2 interface shape, and thus outline the necessity of accurate simulation tools.

INTRODUCTION

Device isolation presents critical aspects for circuit packing density in VLSI. LOCal Oxidation of Silicon (LOCOS) is classically limited by the bird's beak extension and lateral diffusion of the channel-stop region into active transistor area. In order to evaluate new isolation processes (Hui, 1982; Sawada, 1985), numerous technological and device physics aspects have to be investigated to clarify important two dimensional (2D) parasitic effects, and so the use of coupled process/device simulations is of prime necessity.

The IMPACT3 two dimensional device simulator, originally devoted to MOS transistor optimization, has been extended to isolation structure analysis (IMPACT3.2). This newly developed simulation program is automatically linked to the 2D process simulator IMPACT2 (Collard, 1986). In order to demonstrate the efficiency of this simulation system, a comparison between semi and fully-recessed isolation structures is presented and validated by experimental measurements.

DEVICE SIMULATION TOOL

The ease in dealing with non-planar Si/SiO_2 interface and computational time requirements constitute two important criteria for isolation modeling because of the large simulation area. Therefore, in order to take into account the typical nature of isolation structures , the following distinctive features have been developed.

- Depending on bias conditions, either Poisson equation or Poisson and carriers continuity equations are solved by the finite-difference technique together with the box integration method. In the last case, the decoupled resolution strategy is used according to the low current mode of operation implied in this kind of device.

- Special attention has been devoted to the formulation of discretized equations to suit an arbitrary Si/SiO_2 interface. An example of a 20 microns long meshed structure shows the consistency with the oxide shape issued from process simulation (fig. 1).

- A non uniform mesh is automatically generated according to spatial key points such as field oxide boundaries, depth and lateral junctions location.

- The four points discretization scheme leads to a regular filled matrix system that enables the application of an efficient and stable preconditioned conjugate gradient solver.

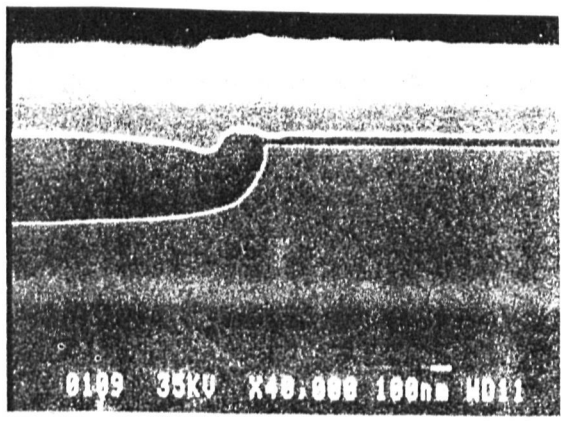

FIG. 1-A : CONSISTENCY BETWEEN EXPERIMENTAL RESULTS, PROCESS AND DEVICE SIMULATIONS. SEM CROSS-SECTIONAL VIEW OF A BURIED SILO ISOLATION STRUCTURE

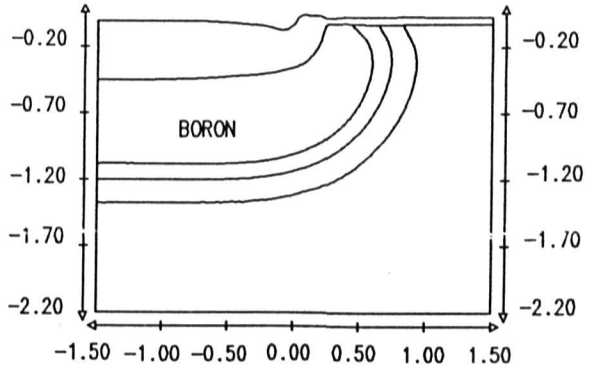

FIG. 1-B : CONSISTENCY BETWEEN EXPERIMENTAL RESULTS, PROCESS AND DEVICE SIMULATIONS. BURIED SILO PROCESS SIMULATION AFTER THE FIELD OXIDE FORMATION.

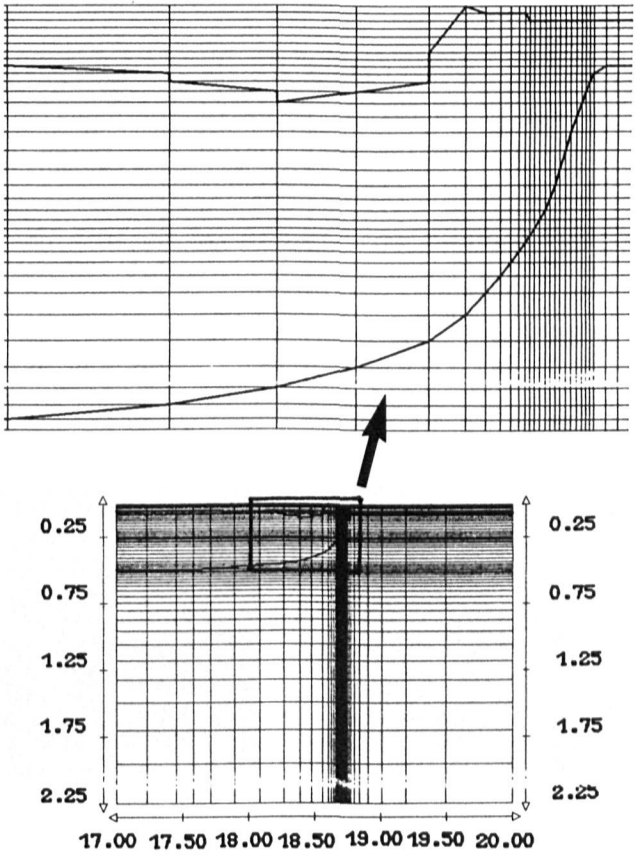

FIG. 1-C : CORRESPONDING DEVICE SIMULATION. A PART OF THE 20 MICRONS LONG STRUCTURE AND A ZOOM OF THE BIRD'S BEAK REGION. THE Si/SiO_2 INTERFACE IS DESCRIBED BY DIAGONAL SEGMENTS BETWEEN TWO MESH POINTS.

APPLICATION AND VALIDATION

Process description

Table I outlines the main characteristics of the isolation structures that have been investigated. SEM cross-sectional views of both structures are shown in fig. 2. For each of them, two versions have been fabricated:

- An aluminium gate version for which a 0.5 micron phospho-silicate-glass (PSG) layer was deposited prior the aluminium level (fig. 3).

- A polysilicon gate version. In this case, the n^+ diffusion regions are self-aligned to the polysilicon. A 550 A° thick oxide layer of about 3 microns long exists between the field oxide mask and the edge of the poly mask (fig. 4).

TABLE I

	Field implant	Field oxidation step	Field oxide thickness	n^+ region implant	Annealing
Semi recessed structure	2 $10^{13}cm^{-2}$ at 25 Kev	1000°C 220 mn	716 nm	5 10^{15} cm^{-2} at 140 Kev	950°C 45 mn
Fully recessed structure	2 $10^{13}cm^{-2}$ at 25 Kev	950°C 370 mn	735 nm	5 10^{15} cm^{-2} at 140 Kev	950°C 45 mn

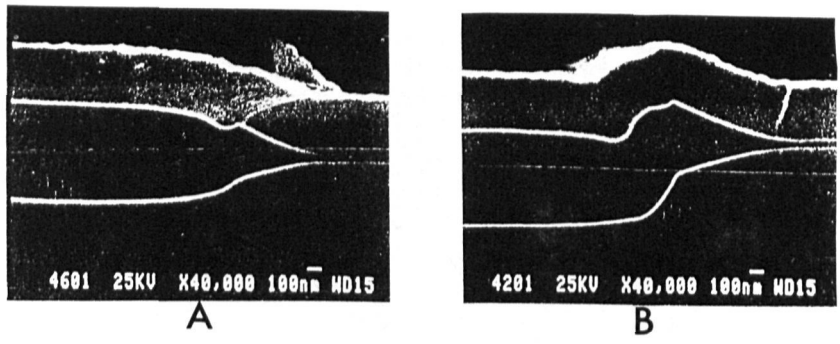

FIG. 2 : SEM CROSS-SECTIONAL VIEW OF THE FIELD EDGE ISOLATION STRUCTURE
(A) SEMI-RECESSED PROCESS (B) FULLY-RECESSED PROCESS

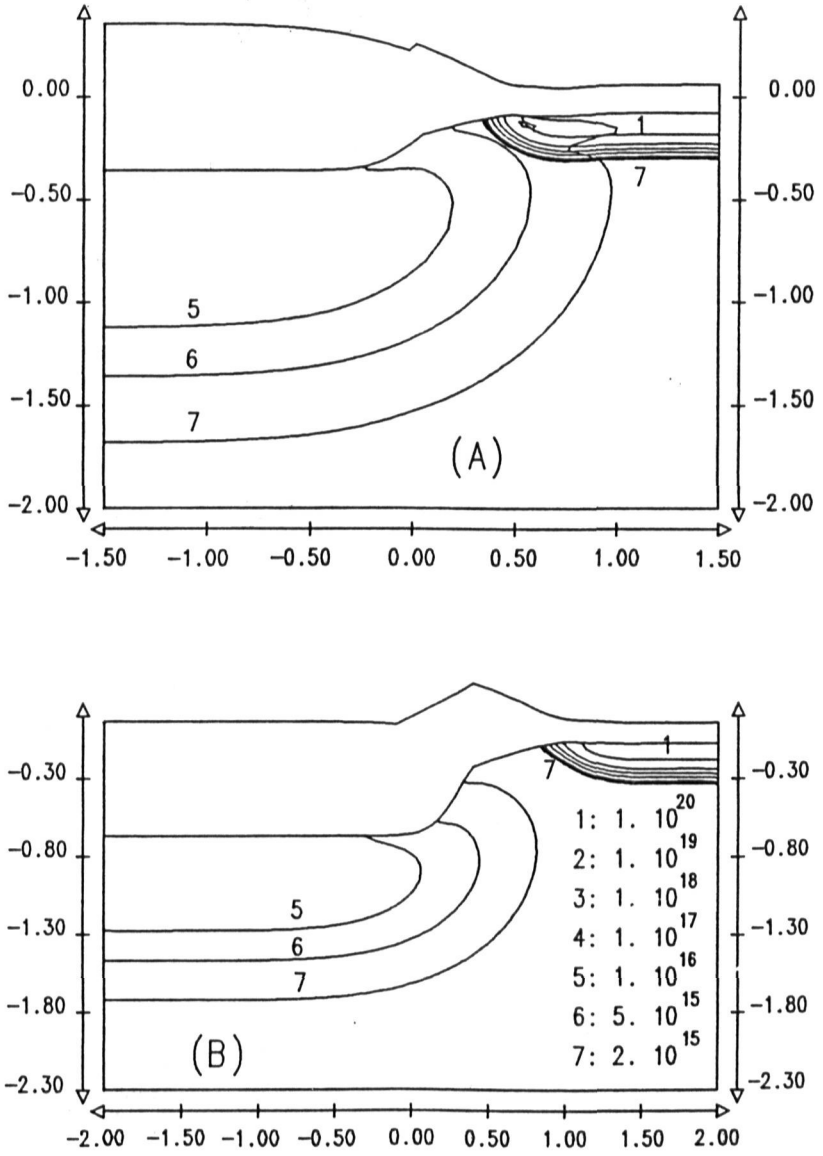

FIG. 3 : ALUMINIUM GATE STRUTURES 2-D IMPURITIES EQUI-CONTOURS LINES
(A) SEMI-RECESSED STRUCTURE (B) FULLY-RECESSED STRUCTURE

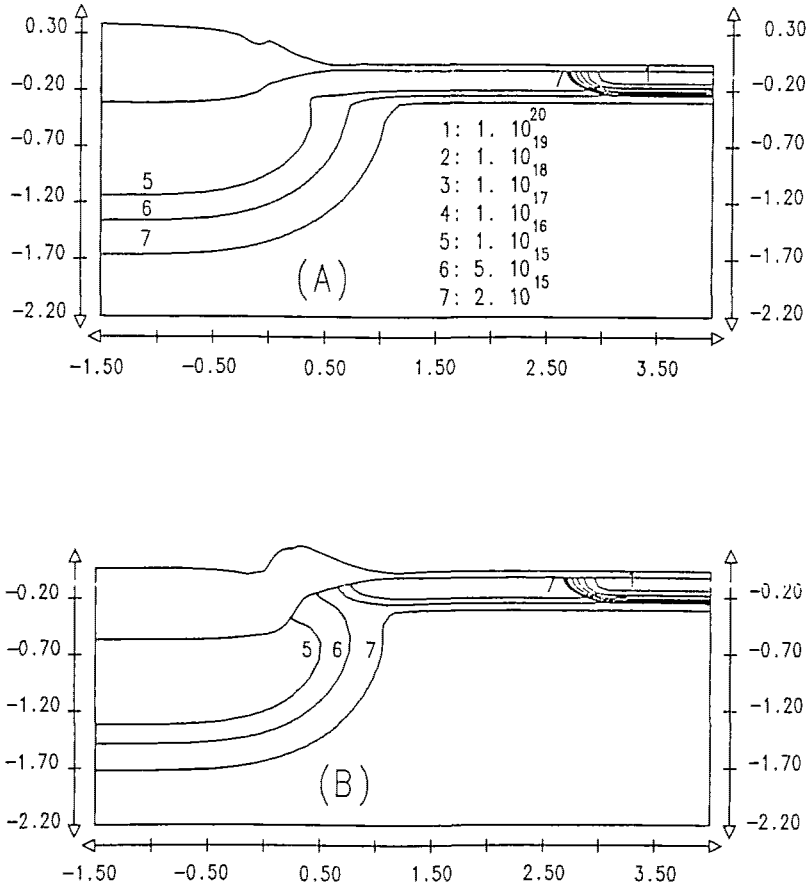

FIG. 4 : POLYSILICON GATE STRUCTURES 2-D IMPURITIES EQUI-CONTOURS LINES
(A) SEMI-RECESSED STRUCTURE (B) FULLY-RECESSED STRUCTURE

Isolation properties

The major difference between the semi-recessed and the fully-recessed structure is the bird's beak shape. The oxide corners incorporated into the channel govern, in such a case, the current flowing in the overall structure, according to different potential barrier deformations. A more pronounced corner shape has tendency to reduce the field effect induced by the gate bias in the silicon region located under the bird's beak, and thus limits the total current. This last result explains the better isolation properties of the full-rox isolation structure compared to the semi-rox one: the ID-VG characteristics for both aluminium gate version (fig. 5) and polysilicon gate version (fig. 6) illustrate this point. An excellent agreement is found between measured and calculated drain currents that validates the simulation approach.

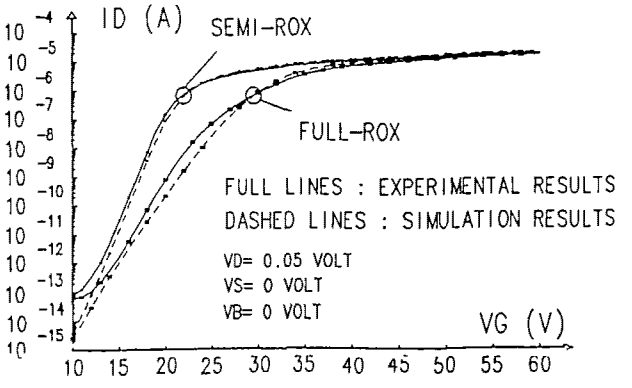

FIG. 5 : ALUMINIUM GATE VERSION
SIMULATED AND MEASURED ID-VG CHARACTERISTICS W/L= 100/20

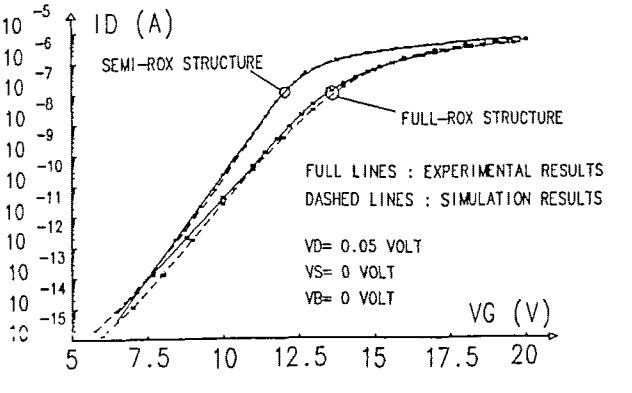

FIG. 6 : POLYSILICON GATE VERSION
SIMULATED AND MEASURED ID-VG CHARACTERISTICS W/L= 100/20

Further simulations have been carried out on 2 and 7 microns long aluminium gate devices without the PSG layer, for a 5 volts drain bias condition. Characteristics plotted in fig. 7 demonstrate the sensitivity of the semi-recessed isolation structure to the n^+ to n^+ spacing (L). By opposition, the fully-recessed structure does not reveal this typical 1/L dependence in the subthreshold mode of operation (Goodwin, 1984). Indeed, the effective channel length is , in this case, reduced to the curved part of the field oxide interface and makes the whole parasitic transistor dominated by the two corner devices.

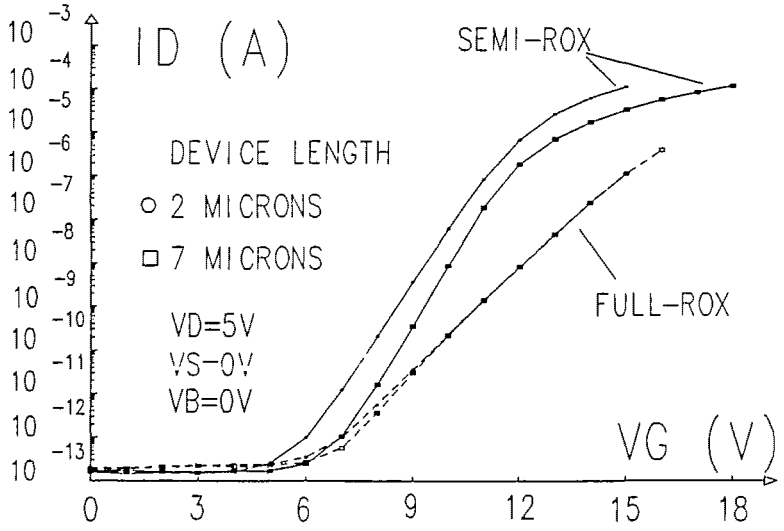

FIG. 7 : CALCULATED ID-VG CURVES FOR DIFFERENT DEVICE LENGHTS
V_{source} = 0 Volt , V_{bulk} = 0 Volt , V_{drain} = 5 Volts

Sensibility to DIBL effect

Simulations performed on two microns long devices have allowed to analyze the effect of Drain Induced Barrier Lowering (DIBL) combined to the corner effect. As the curved part of the interface located on the drain side requires more band bending to invert because of the drain controlled depletion region, the channel is firstly formed in the source region (fig. 8). Fig. 9 illustrates the potential distribution along the interface for gate bias varying from 0 to 15 volts. This result shows how the newly located potential barrier leads to a better immunity against the DIBL effect, for the fully-recessed isolation structure.

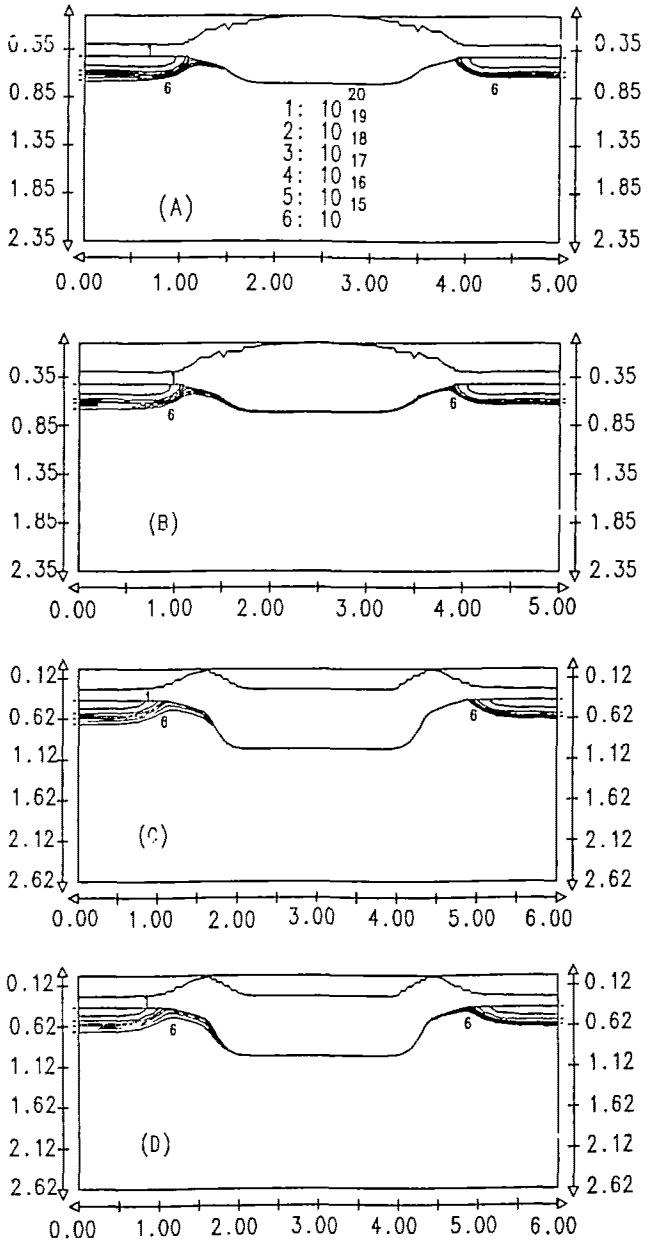

FIG. 8 : ELECTRON DENSITY DISTRIBUTION DURING CHANNEL FORMATION
V_{source} = 0 volt , V_{bulk} = 0 volt , V_{drain} = 5 volts

SEMI-ROX STRUCTURE : (A) V_{Gate} = 5 volts , (B) V_{Gate} = 15 volts
FULL-ROX STRUCTURE : (C) V_{Gate} = 5 volts , (D) V_{Gate} = 15 volts

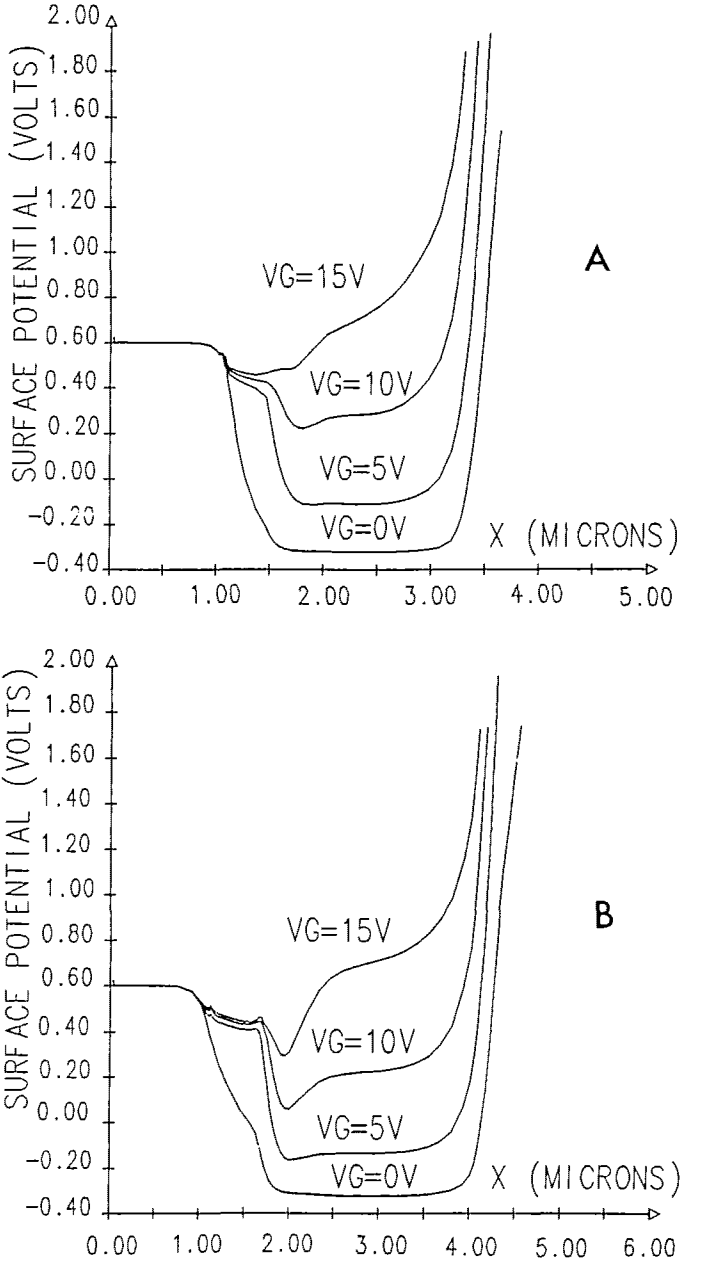

FIG. 9 : POTENTIAL DISTRIBUTION ALONG THE INTERFACE
V_{source} = 0 Volt , V_{bulk} = 0 Volt , V_{drain} = 5 Volts , W= 100 microns
(A) SEMI-ROX STRUCTURE (B) FULL-ROX STRUCTURE

CONCLUSION

The use of a specialized 2D device simulator and the coupling with a 2D process simulation program has been described. The simple but efficient methods, used in this simulation approach, have proved the capabilities to investigate physics of new isolation structures. In particular, the obtained results have revealed a strong dependence of the isolation properties to the field oxide shape.

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