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THE SIMULATION OF FETs CONTAINING SINGLE AND MULTIPLE PLANES OF DOPANT ATOMS

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1 INTRODUCTION

The techniques of Molecular Beam Epitaxy and MOCVD allow for the epitaxial deposition of Silicon, Gallium Arsenide and other related ternary compounds at sufficiently low temperatures that donor and acceptor impurities when incorporated do not diffuse significantly. In addition, the introduction of these impurities can be controlled with sufficient accuracy and speed that single atomic planes of dopant can be deposited.
The use of such 'planes' of dopant in semiconductor device structures has been significant over the last few years, with applications being suggested for new majority carrier rectifying structures(2) transistors(3) balanced mixers(4) and regenerative switching devices(5).

In 1981 a one-dimensional analysis was presented (6) for an FET in GaAs in which the channel impurities were contained in a one-dimensional plane. The plane was treated as having zero thickness, with the electrons travelling in the undoped regions on either side of the impurity plane. The expected linear transfer characteristic was accompanied by a sub threshold exponential region, and the gate capacitance showed a constant region followed by an abrupt reduction at the point where the plane became fully depleted.

A single-plane FET was recently fabricated (7) which exhibited transconductance claimed to be the highest reported for a homostructure GaAs FET, and comparable with selectively doped heterostructure transistors in which the electrons form a 2-dimensional gas with very high mobilities. A number of other advantages are shown for this form of FET, including high gate breakdown voltage and linear current-voltage characteristics.

In this paper the concept of delta-function doping is extended to more than one plane, the focus being on the selective use of analytic and numerical simulation tools in order to ascertain the primary characteristics of such devices.

2 BASIC CONCEPTS

While a single-plane FET lends itself to an analytic solution based on the usual gradual channel approximation and incorporating quantization effects in the v-shaped potential well in the channel, resort has to be made

to 2-D simulation for multiplane operation. For this reason we confine our treatment to the classical drift-diffusion formulation with no quantization or hot electron effects taken into account.

Single, Unconfined Planes

The v-shaped potential well formed by a plane of impurities and unperturbed by any applied bias is described by the following solution of Poisson's equation in which the background impurities are ignored:

$$x = \frac{L_D}{\sqrt{2}} \left(e^{-\frac{U}{2}} - e^{-\frac{U_{om}}{2}} \right) \tag{1}$$

L_D is the intrinsic Debye length and U and is the normalised potential with respect to the intrinsic level. U_{om} is the value of U at the impurity plane. The potential distribution described by (1) is illustrated in Fig. 1, for Silicon and GaAs, together with the electron distribution for the two semiconductors. It is seen that 90% of the electrons are confined in a region 600A˚ on either side of the plane.

When a bias voltage is applied to one side of the plane the potential well becomes asymmetric but with the difference in slopes on either side of the potential well remaining constant through Gauss's Law.

$$\left[\frac{du}{dx}\right]_{o+} - \left[\frac{du}{dx}\right]_{o-} = \frac{q^2 Np}{kT\epsilon_s} \tag{2}$$

If the plane of impurities is confined in one of its lateral dimensions, a 2-dimensional potential well is formed as illustrated in Fig. 2. When this is depleted the depth of the potential well is again reduced with the consequent reduction in the number of electrons present.

3 Single Plane FETs

The simplest model that can be formulated for the single-plane FET is to assume the electrons to be confined entirely to the plane [6]. This leads to the following equation for the drain current per unit of gate width, as a function of applied drain V_D and gate V_g biases.

$$I_D = \frac{q\, N_p\, \mu_o\, v_s}{v_s L_c + q N_p \mu_o^2 V_D} \left\{ \left[1 - \frac{\epsilon_s\, (V_g + \Phi_b)}{q\, N_p d} \right] V_d - \frac{\epsilon_s\, V_D^2}{2q\, N_p d} \right] \tag{3}$$

where N_p is the area density of donors in the channel and a saturating velocity field curve of the form $v = \mu_o E/(1 + \mu_o E/v_s)$ has been assumed,

d is the depth of the plane below the gate and ϕb is the barrier height of the Schottky gate. Eqn. (3) is valid up to pinch off, when

$$V_D = V_{Dp} = \frac{qN_p d}{\epsilon_s} - V_g - \Phi_b \quad (4)$$

Such a formulation gives a first-order description of the transistor characteristic but is unrealistic since it takes no account of the spread of electrons above and below the plane, nor of the change of shape in the v-shaped potential well at different positions along the channel. The former is likely to be important as values of plane depth d in experimental structures are reported to be as low as 300A˚ (7).

The shape of the potential well is symmetric at low drain and gate bias but becomes shallower and more assymmetric as the gate voltage increases. Also with significant drain bias the assymetry increases until at the drain end near pinch off the well becomes more L-shaped.

In the non-quantized model the electron concentration can be readily calculated, for this changing well shape but for a quantized 2-DEG approach the sub-band energy level is a function of well-shape since the De Broglie wavelength is fitted to the well width to find that energy. A more rigorous 1-D formulation can be made where the Debye tails are treated by solving Poisson's equation near the plane and ignoring the background doping. This leads to the following expression for the area density of electrons in the vicinity of the plane in terms of the normalised gate voltage.

$$n_p = N_p - \frac{\epsilon_s kT}{q^2} \left\{ K^2 - 2\frac{\surd 2K}{L_D} e^{\frac{U_o}{2}} + \frac{2}{L_D^2} e^{U_g} \right\}^{\frac{1}{2}} \quad (5)$$

where $K = q^2 N_p / \epsilon_s kT$, U_o is the normalised potential at the plane and U_g the normalised gate voltage. The gate voltage is related to U_o by

$$U_g = \mathrm{Ln} \left\{ \frac{4A\left[\frac{Be^{U_o}}{\surd A} + 1 \qquad -1\right]}{B\left[\frac{Be^{U_o}}{\surd A} + 1 \qquad +1\right]} \right\} - b\surd A \quad (6)$$

where $A = K^2 - 2\surd 2K \exp(U_o/2)/L_D$ and $B = 2/L_D^2$

The relationship between the free electron area density in the plane n_p and the normalised gate voltage Ug can be evaluated by giving values to the parametric variable U_o, and calculating n_p and U_g from (5) and (6). The

result is shown in Fig. 3 for different values of plane depth b. Also included is the dependence of n_p based upon the simplified analysis where the electrons are confined strictly to the plane.

The gate capacitance is related to dn_p/dU_g and will therefore show constant regions falling off abruptly as the plane becomes fully depleted. The value of the capacitance is, of course, higher for shallower planes.

4 NUMERICAL MODELLING OF THE PLANAR FET STRUCTURE

A 2-D simulation of the single plane FET has been carried out using the PISCES device simulator. Here we had to make the following restrictions. First the field-dependent mobility of GaAs could not be used since this led to instability problems and convergence was not possible. Secondly the plane had to be represented by a finite width region with volume doping adjusted to give the appropriate total number of impurities required in the plane. Thirdly, the formulation is restricted at present to drift-diffusion.

Single Plane FETs

The simulated transfer characteristic is shown in Fig. 4 which ignores velocity overshoot, hot electron effects, and quantization. Although PISCES has the capability to simulate trapping phenomena the latter were ignored for the present purposes.

Multiplane FETs

The mesh used for the simulation of a 2-plane FET is shown in Fig. 5 for a gate length of 2 microns. The planes are 1000 and 2000 A˚ below the surface respectively, and are represented by 100 A˚ regions in which the donor concentration is a Gaussian distribution with a peak of 2×10^{18} cm^{-3}. The background doping was 5×10^{16} cm^{-3} and the mobility was taken to be a function of donor concentration only. The transfer characteristic for the 2-plane device is shown in Fig. 6. Two linear regions are observed, the slopes of which are in the ratio of 2:1. Because of the low doping density in the region between the surface and the first plane the latter is partially depleted at zero bias. These two distinct regions imply that the two planes deplete relatively independently of each other, with the upper plane virtually emptying of charge before the lower one is materially affected. Figures 7 to 9 shows a series of potential plots for gate voltages in the range +1V to −5 V for a fixed drain voltage of 1V. The successive depletion of the two planes and their intermediate layers can be clearly seen. The layer above the upper plane must be reasonably highly doped to prevent the built in potential of the gate depleting that plane. However, the layers between the planes and below could have a much lower doping. This would bring the two regions of linear slope closer together providing a sharper transition between them. Thus it can be seen how the transfer characteristic may be tailored by variation of the plane depth, plane doping and intermediate layer doping.

CONCLUSIONS

Characteristics of single and double-plane FETs have been described with a combination of analytic and numerical simulation tools. Concentration of the channel charge in a thin 2-dimensional region leads to a number of advantages.

First the transfer characteristic is linear for small drain voltages and because the electric field distribution between the gate and plane is trapezoidal rather than triangular the gate breakdown voltage will be greater than for the uniformly doped channel device.

Second, the confinement of electrons to a narrow channel leads to the possibility of a 2-D electron gas forming with consequent high mobility. The possibility of achieving this without using heterostructures is attractive because it leads directly to the possibility of it occurring in silicon.

Thirdly, the gate capacitance has been shown to be approximately constant except towards pinch off and this could have advantages in the tuning out of stray capacitances for optimum impedance matching at high frequencies.

For the multiplane FET it has been shown that two distinct regions occur in the transfer characteristic, where the g_m's are in the ratio of the plane depths. The upper plane appears to deplete almost fully before the lower one loses many electrons.

The results presented give only a first-order appreciation of the characteristics of the two-plane FET. There are clear short-comings in the simulation tools used which suggest ways in which they might be developed. These include, within the present context, quantization effects and a well-shape that depends in turn on the free-electron distribution 2-D effects and non-equilibrium transport when the channel length is very short.

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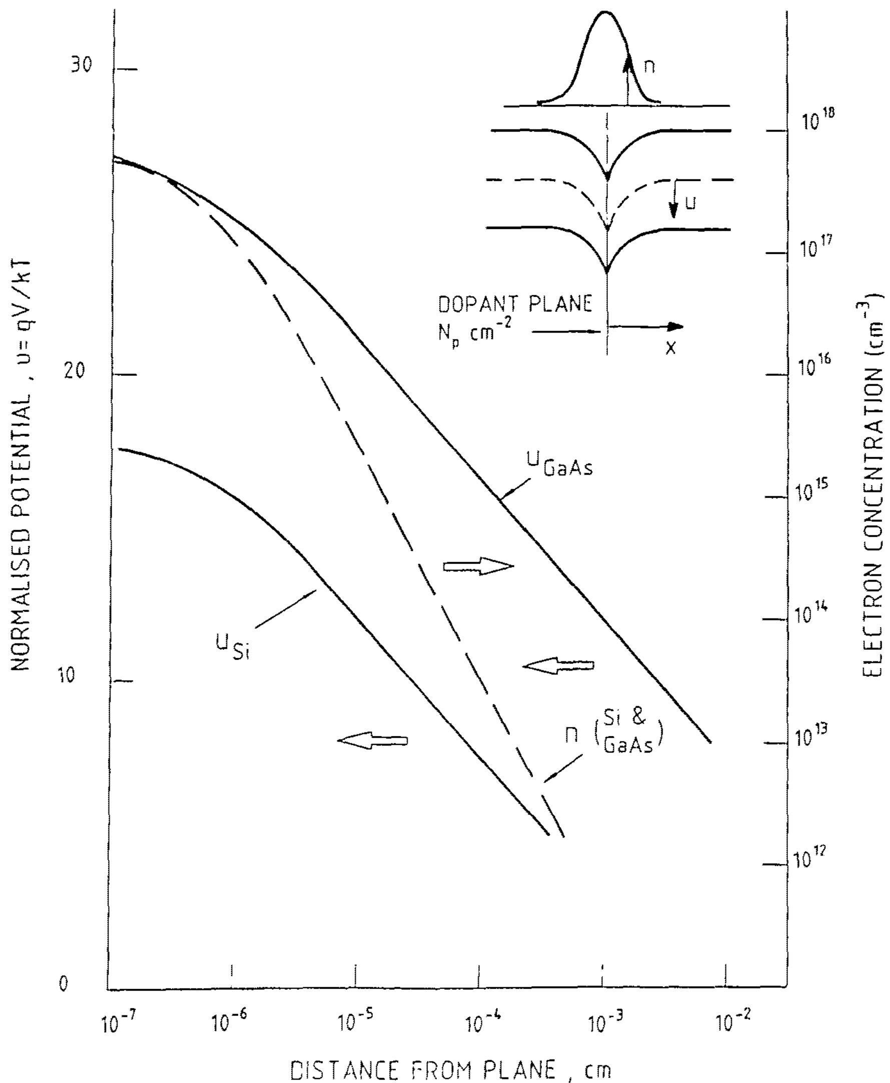


FIGURE 1(a) ELECTRON AND POTENTIAL DISTRIBUTION AT PLANE OF DOPANT $N_p = 10^{12}$

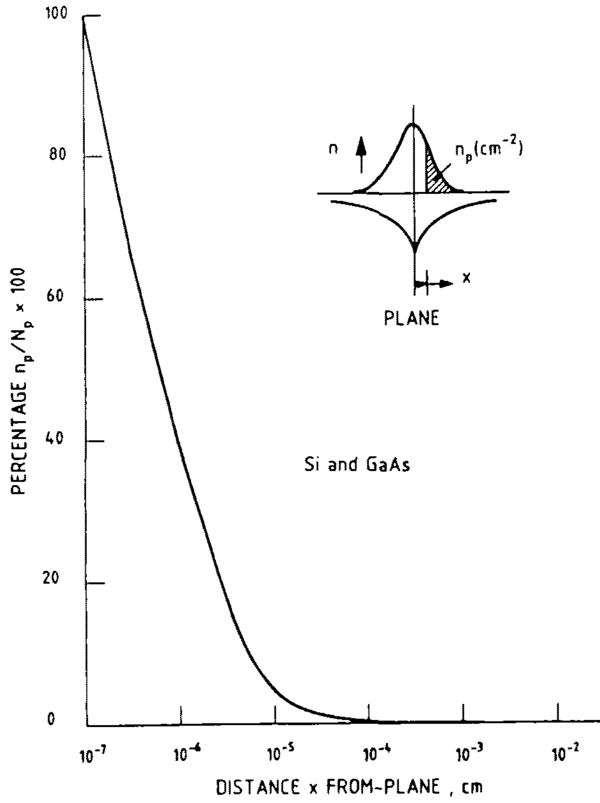


FIGURE 1(b) PERCENTAGE OF TOTAL ELECTRONS NEAR PLANE

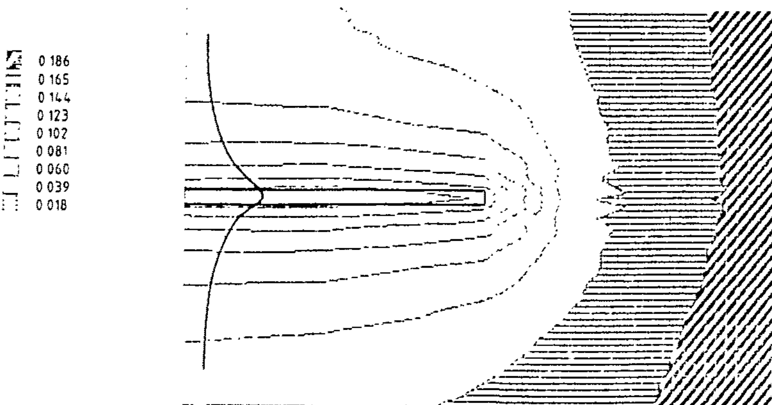


FIGURE 2 POTENTIAL DISTRIBUTION NEAR 2-D PLANE OF IMPURITIES

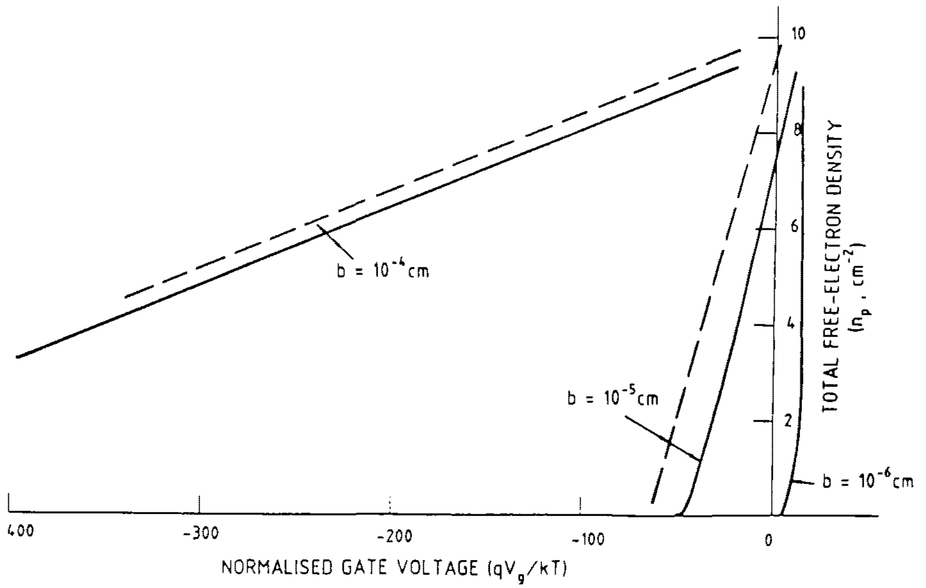


FIGURE 3 ANALYTIC RESULTS FOR SINGLE PLANE FET

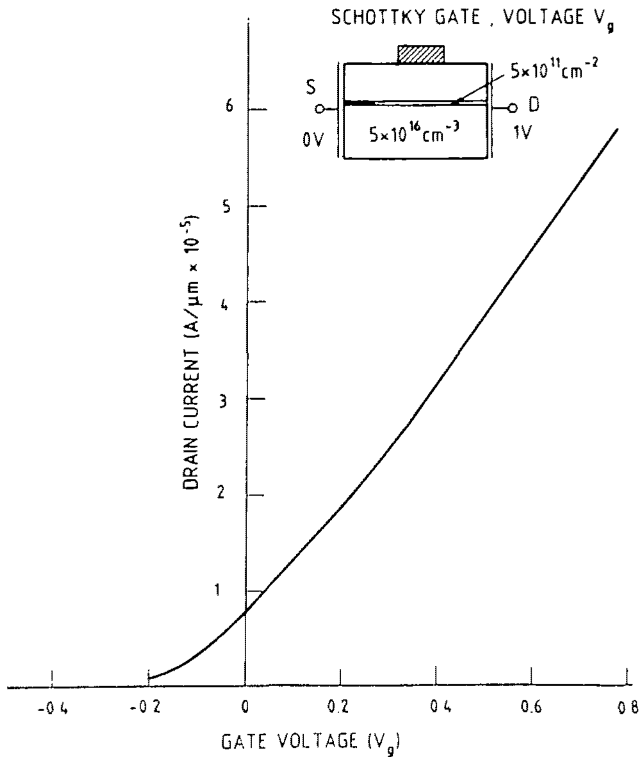


FIGURE 4 TRANSFER CHARACTERISTIC OF SINGLE PLANE FET

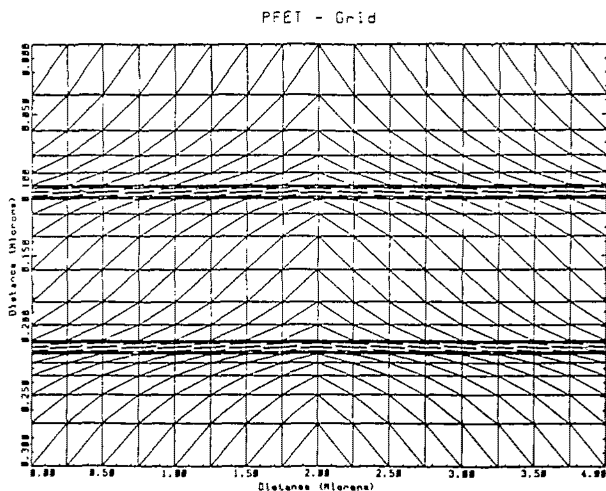


FIGURE 5 PISCES MESH FOR 2-PLANE FET

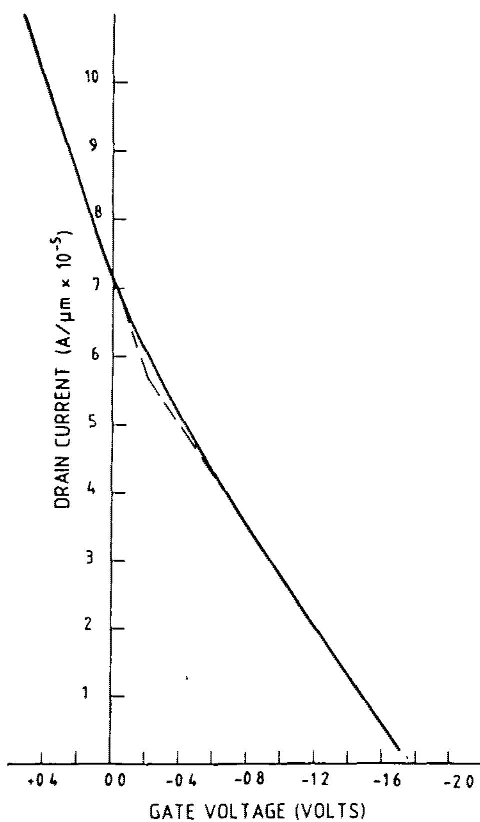
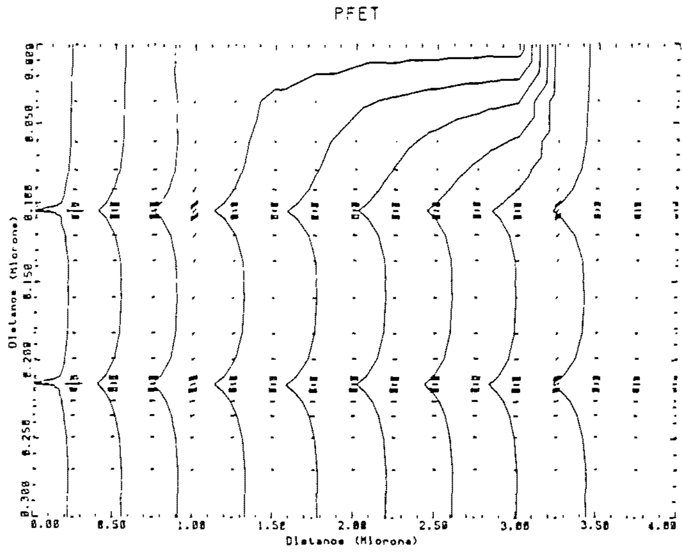
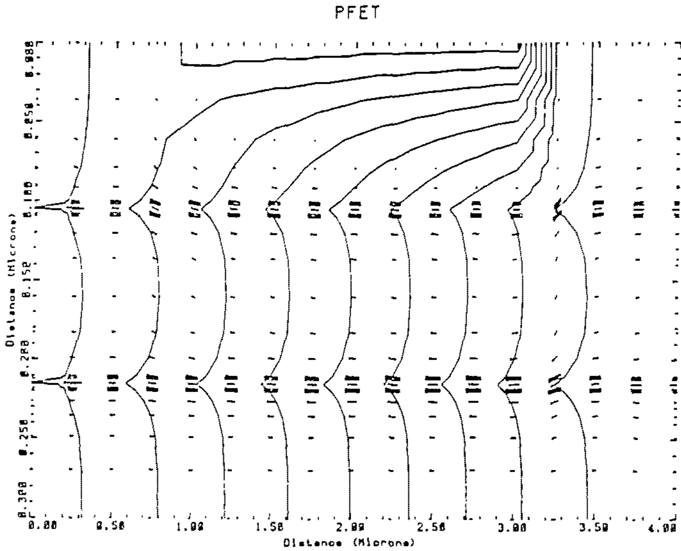


FIGURE 6 TRANSFER CHARACTERISTIC FOR 2-PLANE FET

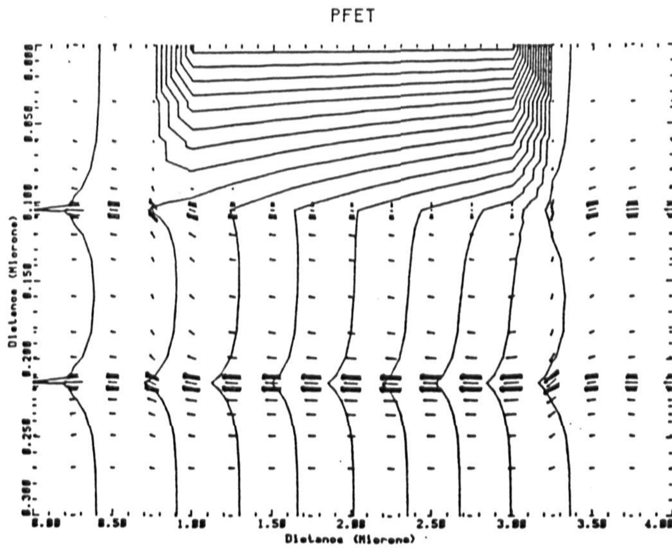


(a) V_G = 1V

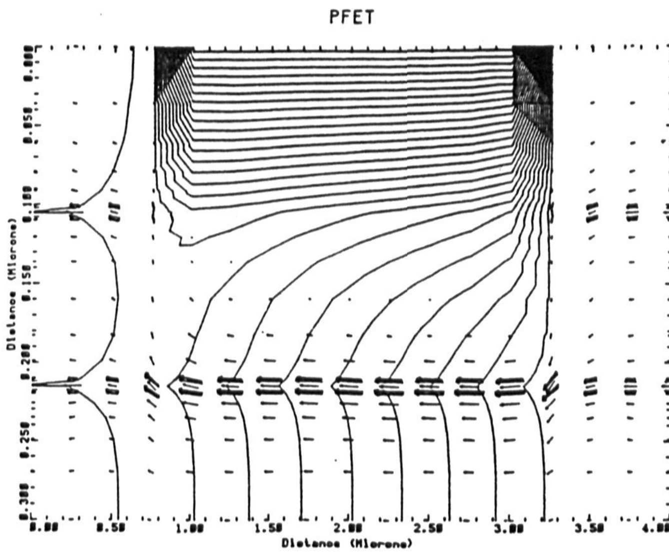


(b) V_G = +0.7V

FIGURE 7 EQUIPOTENTIAL PLOTS AND CURRENT VECTORS FOR 2-PLANE FET

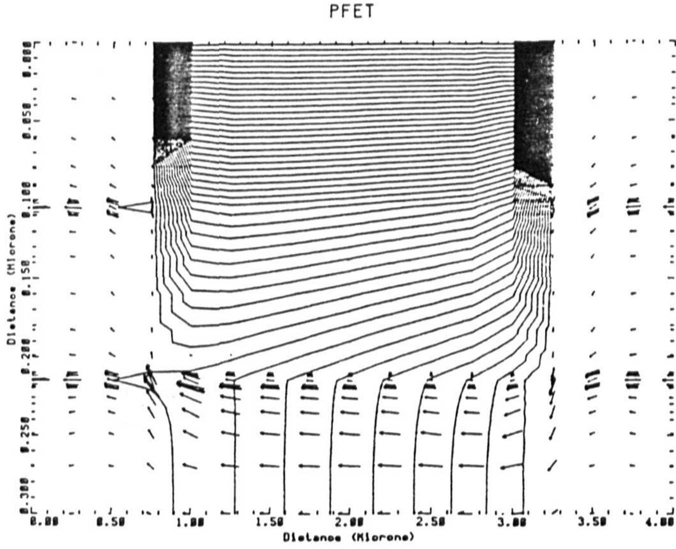


(a) V_G = 0V

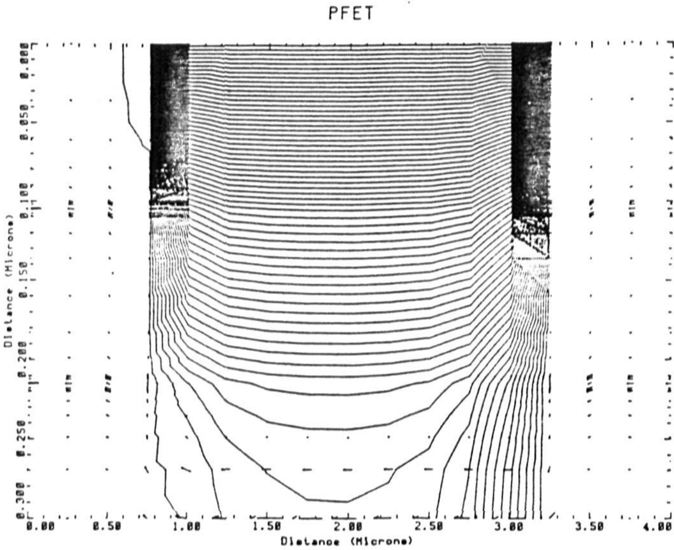


(b) V_G = -1V

FIGURE 8 EQUIPOTENTIAL PLOTS AND CURRENT VECTORS FOR 2-PLANE FET



(a) $V_G = -3V$



(b) $V_G = -5V$

FIGURE 9 EQUIPOTENTIAL PLOTS AND CURRENT VECTORS FOR 2-PLANE FET