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Computer Simulations of Parallel-to-Series Conversion in Solid State Frame Transfer Image Sensors

J. Bisschop

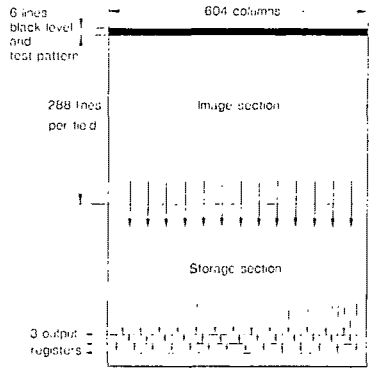
Philips Research Laboratories
P.O. Box 80.000, 5600 JA Eindhoven, The Nehterlands

Abstract

In developing a solid state image sensor without the problems of incomplete charge transfer or insufficient charge handling capacity it is necessary to simulate the electrical behaviour of the device. We perform these simulations using a 3D off-state and a 2D on-state semiconductor simulation package. The use of a 3D package is necessary because of the complicated structure of the device. As an example of the application of these simulations the calculation of charge transfer efficiency in the parallel-to-series conversion in a frame transfer image sensor is explained.

Introduction

The frame transfer image sensor is a type of sensor in which the whole image area is sensitive to light. It consists basically of three sections: image, storage, and read-out section (see Fig. 1). The principle of operation is as follows. Photons incident on the image section generate electron-hole pairs in the bulk of the silicon. The electrons are collected in each pixel under positive electrodes, while the holes are drained off. The image and storage section consist of parallel running vertical CCD registers. Charge packets integrated in the pixels of the image section are transported quickly through these CCD registers to the storage section. After that a new field is integrated, while the storage section is read out line by line. The horizontal read-out register consists of three parallel CCD registers to allow a high pixel density at relaxed design rules. The lines are read out from the horizontal registers at the proper video frequency. All registers are bulk n-channel CCD registers.



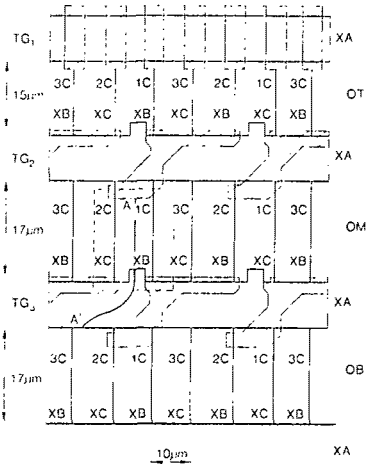


Fig. 1. Schematic representation of the frame transfer image sensor.

Fig. 2. Output register of the image sensor. The shaded areas are channel stop (SP) regions. 1C, 2C, 3C indicate the three phases of the horizontal read-out register. XA, XB, XC are the first, second, third poly-Si layer respectively. Vertical charge transport during parallel-to-series conversion occurs preferentially along the line A-A'. The dashed lines indicate the area used in the simulation of Fig. 3.

The charge packets contain at most about 200,000 electrons. The sensitivity is limited by noise which amounts typically to 20 to 70 electrons. So, the sensor is an analog device which must be able to handle very large as well as very small charge packets. This places high demands upon the accuracy of device simulations. All sensors are designed with the help of computer simulations in order to prevent problems with charge storage and transfer of charge packets.

Due to the small scale of the details of the device 3D calculations are necessary to obtain reliable results. Furthermore, it is necessary to have the possibility of performing on-state (transient) calculations in order to study charge transport. We have at our disposal the packages Paddy (3D off-state) and Curry (2D on-state) (Polak, den Heyer, Schilders, 1987).

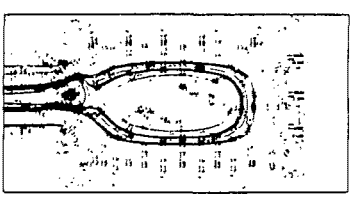
In the next section the use of these packages will be demonstrated on the basis of a problem in the parallel-to-series conversion at the transition from the storage section to the horizontal read-out register.

Parallel-to-series conversion

A part of the transition between the storage section and the horizontal read-out register is shown in detail in Fig. 2. In the image and storage sections the vertical CCD registers are shifted in parallel. In the horizontal read-out register the pixels are read out serially.

Charge packets in vertical channels debouching into 1C are transported down to the bottom register (OB) through OT, TG2, OM, and TG3 registers. The packets above 2C are transported to OM and the packets above 3C stay in the top register OT. After that the packets are transported in parallel in the three registers.

The structure which provides this conversion is rather complicated. The ionized dopants together with the voltage differences between the electrodes create electric fields for the transportation of charge in the horizontal as well as in the vertical direction. Moreover, the ionized dopant atoms create a potential distribution perpendicular to the surface of the device. Therefore 3D simulations are necessary.



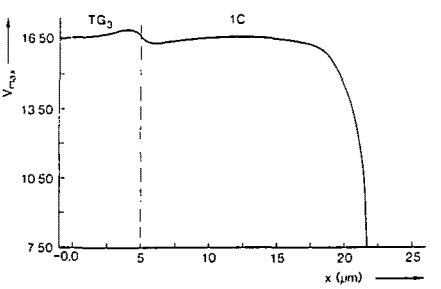


Fig. 3. Contour map of the channel potential under the 1C electrode. There is a large potential well under 1C and a small one under the TG lip.

Fig. 4. Channel potential along the direction of charge transport from 1C to TG3.

One of the problems encountered in parallel-to-series conversion is imperfect charge transfer from 1C to TG3 (or TG2). The effect of such an imperfect-ion is that charge from OB stays behind in OM or OT, leading to dark and bright vertical stripes in the displayed image. The problem is due to a potential barrier near the TG entrance. The barrier is caused by the p-type channel stop regions. Fig. 3 shows a contour map of the channel potential (= potential at depth of charge transport) under the 1C electrode. The map was obtained from 3D Paddy calculations. The figure shows a potential barrier near the TG entrance. The barrier can only be found with 3D calculations. Fig. 4 shows a plot of the channel potential along the line of charge transfer A - A′ in Fig. 2. It is not possible to make the barrier disappear by raising the TG voltage.

On-state calculations

There are several ways to solve the problem. We shall mention and elucidate a few possibilities.

(i) Shorten the IC electrodes. This increases the driving electric field from IC to TG, and hence lowers the barrier.

(ii) Enlarge the lip of the TG electrodes. The lip serves to reduce the potential barrier and to draw electrons under TG. Both methods limit the charge handling capacity of the horizontal registers. Therefore, the maximum amount of charge which can be held under the IC electrodes has been calculated with Paddy.

(iii) Reduction of the SP implant reduces the repulsive action of the channel stop regions and consequently results in reduction of the barrier.

In order to determine what demands a solution must satisfy we must know what potential barrier height still yields undisturbed charge transfer. It is clear that no barrier is the best case, but this turned out to be hardly feasible in practice if we wish to allow a certain degree of misalignment. Therefore we studied charge transport over such a barrier with the 2D on-state package Curry. From 3D calculations the channel potential along the line of charge transfer (A - A'

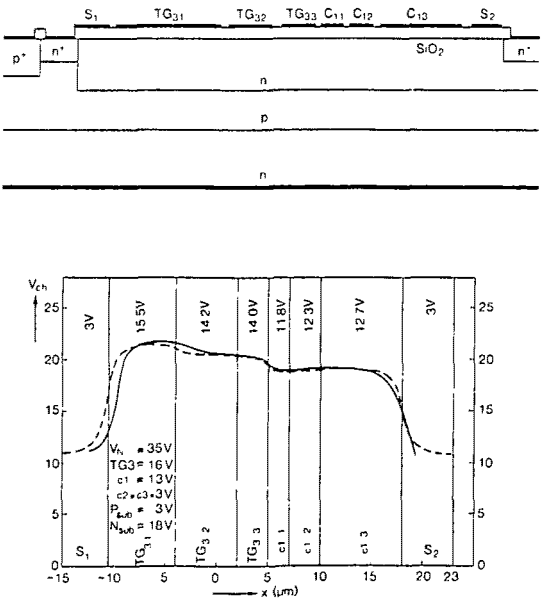


Fig. 5. Input structure for the 2D on-state calculations. The thick lines indicate metal electrodes. The electrodes TG3 and IC have been divided into three parts.

Fig. 6. Channel potential along A-A' (Fig. 2) from 3D (—) and 2D (- -) off-state calculations.

in Fig. 2) was determined. This region was then used as input region for Curry (see Fig. 5). In the 2D model n-contacts have been added on both sides, while a p-contact is on one side only. Furthermore, two switching electrodes S1 and S2 have been added to isolate the 1C - TG region from the contacts. In order to obtain the right channel potential everywhere, the electrodes 1C and TG were devided into three parts each. The potentials on these electrodes were adjusted such that the 2D off-state calculations produced a good fit to the results from Paddy (see Fig. 6). The height of the potential barrier can be adjusted with the electrodes TG33 and C11.

The 2D on-state calculations are rather complicated. In the first run all potentials are set to 0 V. In the second (transient) run the holes have to be removed by driving them to the p-contact. After that the electrons are removed by the n-contacts, except for a certain amount of charge which stays under 1C. This is the starting situation for our on-state calculations. The switches S1 and S2, and TG are negative, while 1C is positive. The next transient takes TG to a positive voltage. Charge flows over the potential barrier from 1C to TG. Depending on the barrier height a certain amount of charge stays under 1C. 1C goes negative in a transient after 200 ns. Most of the rest charge is driven to TG. The results are shown in Fig. 7.

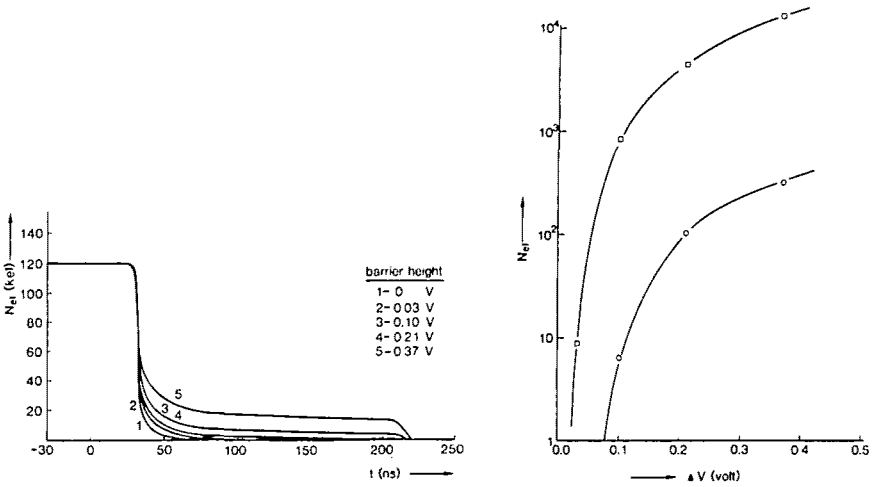


Fig. 7. Charge transfer from 2D simulations for different barrier heights. At t = 0 TG3 goes positive. At t = 200 ns 1C goes negative within 20 ns.

Fig. 8. Rest charge in 1C as a function of barrier height from 2D calculations.
(□) start of 1C transient (t = 200 ns).
(○) end of 1C transient (t = 220 ns).

In Fig. 8 we show the rest charge at the onset and at the end of the last transient. The electrons which are still under 1C at the moment this electrode becomes negative, can go to the neighbouring 2C and 3C electrodes and cause

the vertical stripes. From Fig. 8 we find that less than 10 electrons stay under IC if the barrier height is less than 0.1 V. In view of the noise level of 20 - 70 electrons we state that a barrier height < 4 kT is acceptable in this case. Fig. 9 shows typical experimental curves found in a sensor which exhibited vertical stripes. Deviations from the form of the curves in Fig. 7 are thought to result from the 2D character of the on-state simulations, in which the effect of a narrow entrance is neglected.

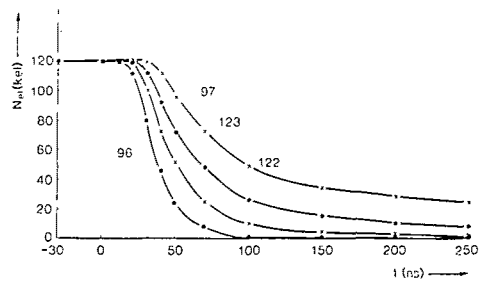


Fig. 9. Experimental number of electrons in IC as a function of time for four different IC cells. Here IC does not go negative at $t = 200$ ns.

Solutions

The solutions which were tried in practice are shortening of the C electrodes and reduction of the shallow p-implant. Simulations predicted a slightly better performance for the latter solution. This was also found in practice. Sensors with a reduced p-implantation were free of vertical stripes.

Conclusions

In view of our results we can state that

(i) the complicated structure of the parallel-to-series conversion in frame transfer image sensors necessitates the use of 3D simulations.
(ii) in order to simulate charge transport in CCD registers with potential barriers in the channel it is necessary to use an on-state simulation package.
(iii) the essential properties of parallel-to-series conversion in frame transfer sensors can be modelled properly with 3D off-state and 2D on-state simulation packages.

Reference

Polak S.J., C. den Heijer and W.H. A. Schilders (1987). Semiconductor device modelling from the numerical point of view. *International Journal for Numerical Methods in Engineering*, Vol. 24, pp. 763-838.