TRANSIENT SIMULATION OF MOSFETS

M. Razaz and S. F. Quigley
Department of Electronic and Electrical Engineering,
University of Birmingham, UK.

SUMMARY

Considerable research has been carried out in the past on the development of fairly accurate steady state models for small size MOS devices. These models are, in general, not capable of dealing with the device switching and AC characteristics. This paper presents a transient model which can simulate accurately both transient and steady state behaviour of micron and submicron MOS devices in two space dimensions. The model has been implemented in a flexible and user-friendly simulator which can easily handle both planar and non-planar MOS structres. typical simulation results for the transient response of such devices are presented and discussed.

1 INTRODUCTION

MOS technology over the past two decades has been characterized by a steady reduction of the minimum device feature size. Due to the inherent two- or three-dimensional geometry of such devices and complicated interacting internal mechanisms involved, even sophisticated analytical models, which require practical characterization of many parameters, fail to predict the device behaviour accurately. Thus numerical simulation becomes a necessity for accurate prediction of the device static and dynamic characteristics.

In the past, considerable effort has been put into the development of reliable and accurate steady state numerical models of MOS devices. The extent of this work has been indicated in recent review papers [1,2]. However, such models can only reveal the DC behaviour of a MOSFET. Transient modelling is necessary for the determination of AC and dynamic characteristics and also for investigating transient breakdown mechanisms such as parasitic bipolar

action in MOSFETs and parasitic thyristor action in CMOS structures.

Comparitively little work has been done on transient modelling of MOS devices [3,4,5]. The model in [3] employs stream functions and those in [4,5] are based on the finite difference approach, and cannot deal effecitively with non-planar MOS devices which are used in today's VLSI technology. This paper presents an accurate two-dimensional transient model for a MOSFET. The potential and charge distributions within the device, and hence the contact currents, at any instant in time are determined by solving the time-dependent Poisson and continuity equations subject to appropriate initial and boundary conditions. A triangular-based finite element method is used for space discretization and the Crank-Nicolson method for time domain solution. Care has been taken to use appropriate generation mechanisms as well as a physically meaningful mobility model that takes account of the electric field, doping density, temperature, and various scattering mechanisms. The transient model has been incorporated into a user-friendly simulator [6] which has its own preprocessor, mesh generator and postprocessor. The latter performs various postprocessing tasks, such as current and field calculation, DC or AC analysis and graphical display of device behaviour in one-, two- or three-dimensional forms.

Transient simulation of an MOS device tends, in general, to be computationally expensive. Therefore much effort has been spent on making the model efficient for a given device, firstly by using justifiable approximations, secondly by using a flexible grid with combined coarse and refined meshes and finally by employing fast direct-solution algorithms with bandwidth reduction facility. The accuracy of the model has been tested against published MOSFET results that have been obtained by an entirely different steady state approach. The agreement has been found to be good. Typical computed results are presented for the transient response and DC threshold characteristic of two short-channel planar and recessed nMOS transistors.

2 THE TRANSIENT MODEL

To develop a transient model for a MOSFET, it is necessary to find the potential and charge distribution within the device at any instant of time. This information can then be used to derive instantaneous contact currents and hence the dynamic response to an input excitation. The potential ψ, for a given charge distribution, can be determined from the Poisson equation:

$$\nabla . \epsilon \nabla \psi = q (n - p - N) \tag{1}$$

where N is the net doping profile and ϵ the Si or SiO_2 permittivity. n and p are the electron and hole densities, which can be found from the continuity equations:

$$q \frac{\partial n}{\partial t} = \nabla . J_n - qR \tag{2}$$

$$q \frac{\partial p}{\partial t} = - \nabla . J_p - qR \tag{3}$$

The individual and total current densities are given by

$$J_n = - q (n\mu_n \nabla \psi - D_n \nabla n) \tag{4}$$

$$J_p = - q (p\mu_p \nabla \psi + D_p \nabla p) \tag{5}$$

$$J_T = J_n + J_p - \epsilon \nabla \frac{\partial \psi}{\partial t} \tag{6}$$

The symbols in (2)-(6) have their usual meanings. Since the current densities are directly dependent on mobilities and diffusion coefficients, it is important that they are modelled accurately. Mobilities and diffusion coefficients are affected by lattice impurity scattering, carrier heating due to electric fields, and surface roughness scattering due to the Si-SiO_2 interface. In the vicinity of the interface, the mobility of the carriers is also modified by quantum mechanical effects due to the extremely narrow potential wells. The models used for mobilities and diffusion coefficients of carriers in the bulk and at the interface are similar to those in [7,2].

The net recombination rate R is, in general, given by

$$R = R_{II} + R_{SRH} + R_{SURF} + R_{AUG} \tag{7}$$

where R_{SRH}, R_{SURF} and R_{AUG} are the Schockley-Read-Hall, surface, and Auger recombinations and R_{II} represents the impact ionization.

The expression used for R_{SRH} is

$$R_{SRH} = \frac{np - n_i^2}{\tau_n(p+p_t) + \tau_p(n+n_t)} \qquad (8)$$

where n_i is the intrinsic concentration, τ_n and τ_p the electron and hole lifetimes, and n_t and p_t the trap levels, which are assumed to be equal to n_i. The doping dependence of τ_n and τ_p are taken from [9]. For the recombination at the MOS interface, τ_n and τ_p in (8) are replaced by the inverse of the electron and hole surface recombination velocities.

R_{AUG} and R_{II} are represented by the following expressions:

$$R_{AUG} = (c_n n + c_p p) (np - n_i^2) \qquad (9)$$

$$R_{II} = -q|J_n|\alpha_n - q|J_p|\alpha_p \qquad (10)$$

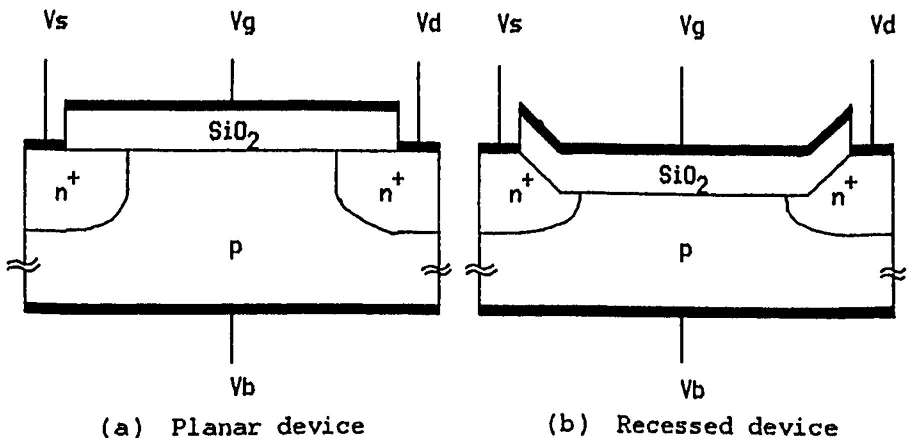
where c_n and c_p are the Auger capture coefficients [8] and α_n and α_p the impact ionization coefficients [10].

To compute ψ, n and p distributions within the device, and hence to obtain a complete model of the device behaviour, equations (1)-(3), together with their auxiliary equations are solved at each timestep sequentially using efficient LU decomposition algorithms. The time scheme is handled by employing the Crank-Nicolson method [11]. An alternative method is to linearize the matrix equations and to solve them simulataneously using a full implicit time scheme. Although the latter approach has a faster convergence and its use may be mandatory for large drain biases when a steady state approach is employed, it requires at least three times more storage which can be problematic for computers with small core memory. A number of assumptions can be made to reduce the computational effort needed for modelling a MOSFET using the sequential approach. An obvious simplification is to ignore the solution of the majority carrier continuity equation by assuming that the quasi-Fermi level of the majority carriers is flat across the device. This simplification is acceptable for steady state calculations, provided that impact ionization is negligible. However, it is not so useful for modelling of transients, during which appreciable substrate current flows, and it cannot give an accurate model of avalanche breakdown. Solving the minority carrier continuity equation in one dimension along the Si-SiO_2 interface, rather than two-dimensionally, can

also save computing time. The timestep of the Crank-Nicolson method, and hence the overall solution time is directly affected by the local dielectric relaxation time. This restriction may become severe in a MOSFET, due to the heavily doped source and drain regions and the sudden increase of the channel charge density caused by a large applied gate bias. To alleviate this restriction and to speed up the solution time, the heavily doped regions of the source and drain diffusions may be modelled by Dirichlet boundary conditions. This has the effect of partially reducing accuracy, but a considerable gain in speed justifies its use.

3 SIMULATION RESULTS AND DISCUSSION

The two structures modelled are shown in fig. 1a and 1b. The first is a planar n-channel MOSFET of 0.8 μm gate length, 0.1 μm oxide thickness and 0.2 μm junction depth. The device length is 1 μm and the substrate doping is 10^{15} cm^{-3}. The gate material is aluminium, giving a flat-band voltage of -.88V. The second is a similar device but with its channel recessed by 0.1 μm. The doping profile of the planar device is shown in fig. 2. It corresponds to an annealed phosphorus ion implantation into a constantly doped substrate. The doping profile of the recessed device is similar. The recessed channel is normally introduced to minimize the threshold voltage shift that occurs in short-channel MOSFETs due to the penetration of the drain field into the channel region. The effect of the recess is to reduce the effective junction depth of the drain diffusion and thus decreasing its influence on the channel.



(a) Planar device (b) Recessed device

Fig. 1 MOS structures modelled

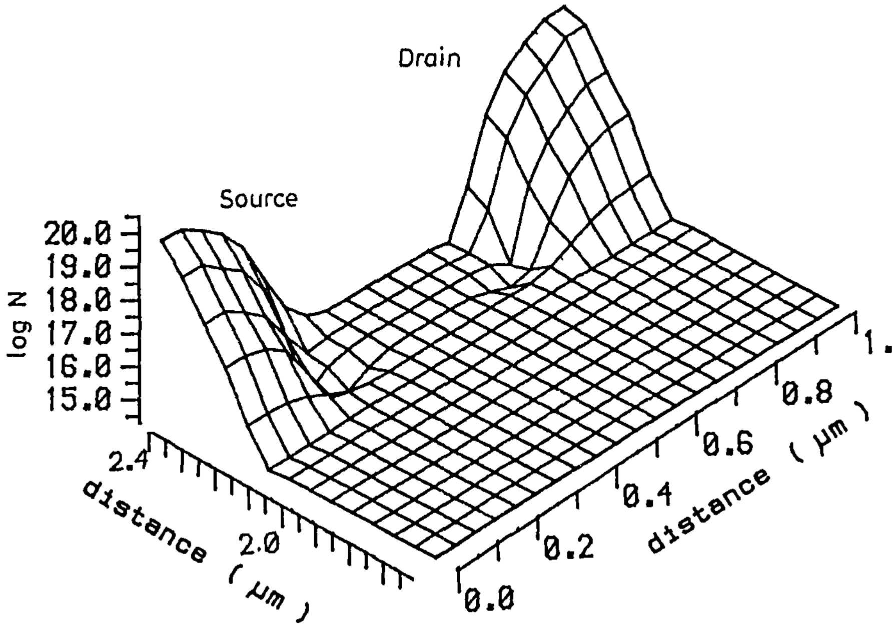


Fig. 2 Doping profile used for planar device

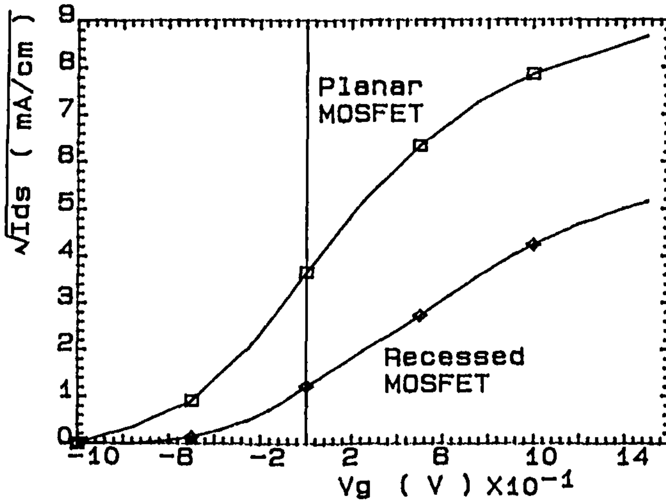
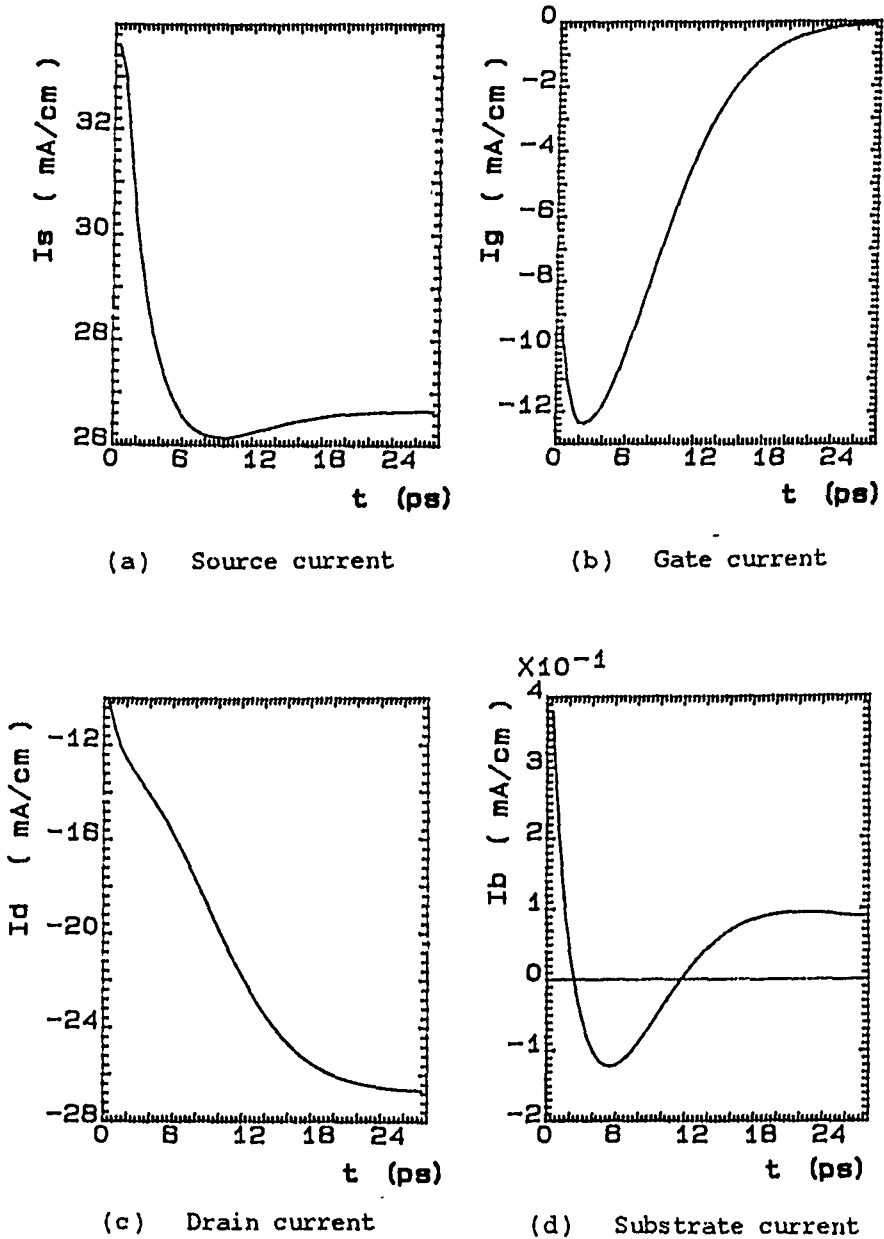


Fig. 3 Threshold characteristics of the planar and recessed nMOS devices shown in fig. 1

The DC transfer characteristics of both structures are presented in fig. 3, which shows that both devices are normally-on and that the threshold voltages are approximately -0.6V for the planar and -0.4V for the recessed structure. The transconductance of the recessed device is lower than that of the planar device by approximately a factor of four. This is due to the smaller amount of charge under the gate in the recessed case.

Fig. 4 shows the transient response of the planar device to a step in gate bias from 0V to 0.25V at V_{ds} =0.5V. Fig. 4a-4d present the source, gate, drain and substrate currents respectively. The conduction and displacement components of the source, drain and substrate currents are also presented separately in fig. 5. The contact currents in each case takes about 30 ps to reach a steady state, and the characteristic consists of two distinct phases. The first, which lasts about 5 ps, is characterized by a strongly enhanced substrate current, corresponding to a strong flow of electrons from the source into the channel, and a diminished drain current, corresponding to a reduced flow of electrons from the channel into the drain. This phase of the transient is the period during which an extra charge under the gate builds up. It co-incides with the peak of the flow of displacement current into the gate. The second phase is characterized by an almost constant source current and a slow fall in the gate current, matched by a slow rise in the drain current. This phase corresponds to the redistribution of potential along the newly enhanced channel. The form of the substrate current characteristic is interesting, changing sign twice during the transient. This is due to the opposing flow of positive conduction current, associated with positive charge being forced out of the device by the increased gate field, and negative displacement current, due to the redistribution of electric fields within the device.

The corresponding results for the recessed-channel device are shown in fig. 6. The form of the transients is much the same, but the planar device switches almost three times as fast as the recessed-channel device. This difference in speed is caused by the penetration of the drain field into the channel region, which lowers the gate capicitance to a much greater extent for the planar structure.



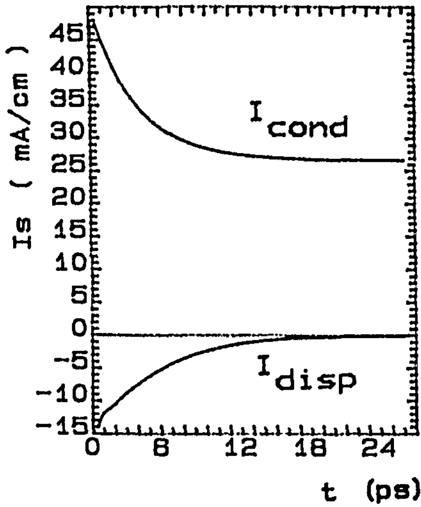
(a) Source current

(b) Gate current

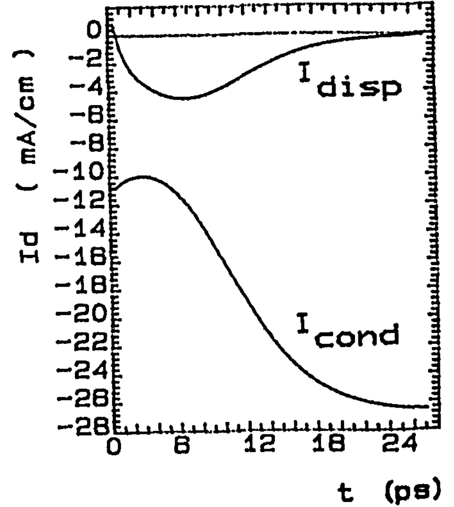
(c) Drain current

(d) Substrate current

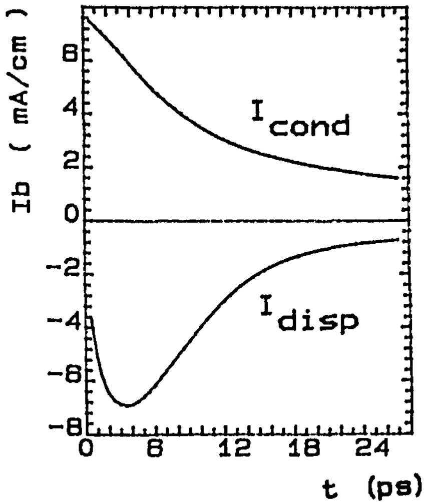
Fig. 4 Contact current transients of the planar nMOS device for a step change in gate voltage from Vgs=0V to Vgs=0.25V



(a) Source current components

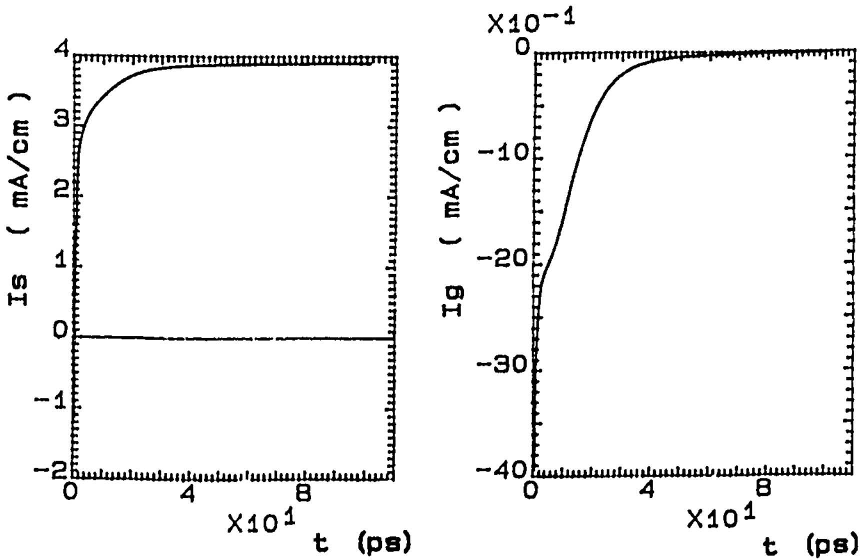


(b) Drain current components

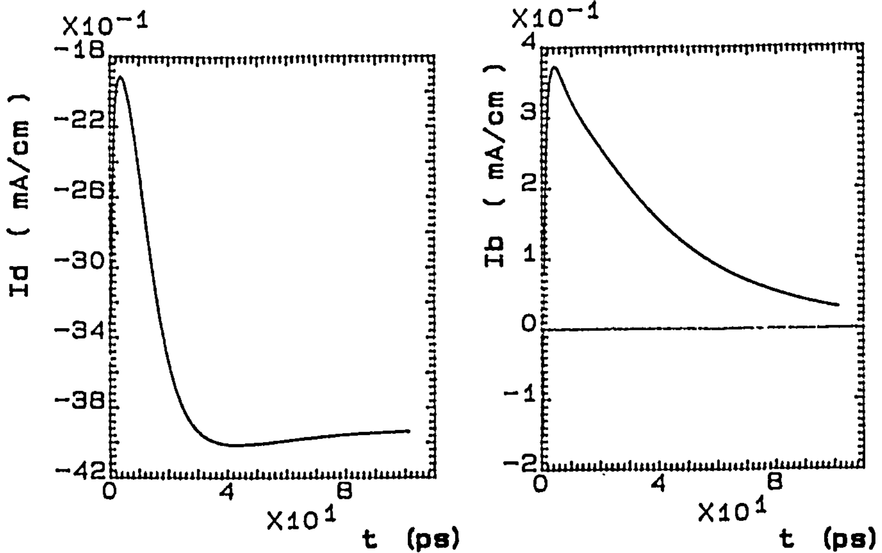


(c) Substrate current components

Fig. 5 Conduction and displacement components of contact current transients for the planar nMOS device

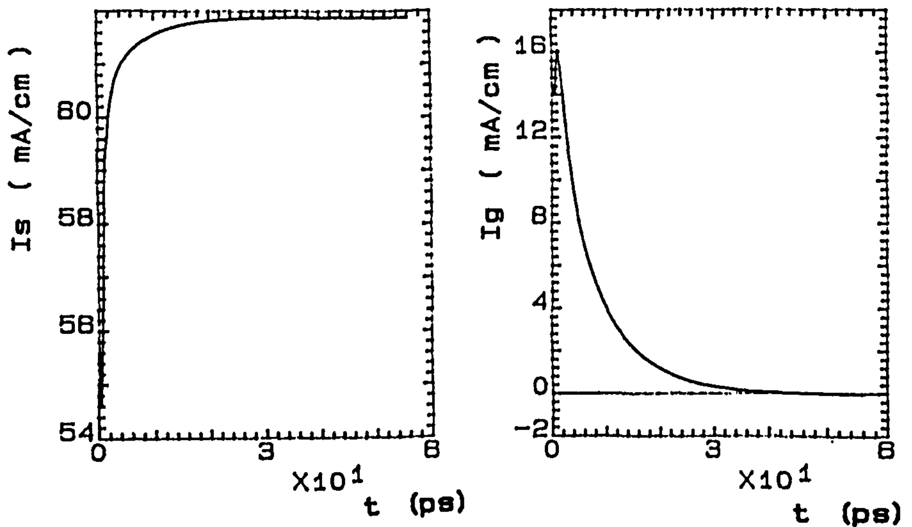


(a) Source current (b) Gate current



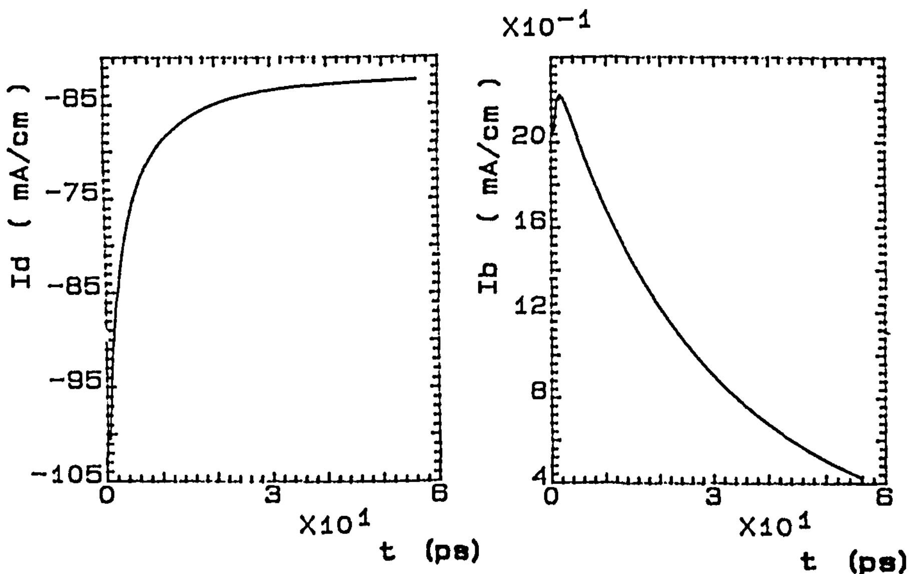
(c) Drain current (d) Substrate current

Fig. 6 Contact current transients of the recessed nMOS device for a step change in gate voltage from Vgs=0V to Vgs=0.25V



(a) Source current

(b) Gate current



(c) Drain current

(d) Substrate current

Fig. 7 Contact current transients of the planar nMOS device for a step change in drain voltage from Vds=0.25V to Vds=0.5V

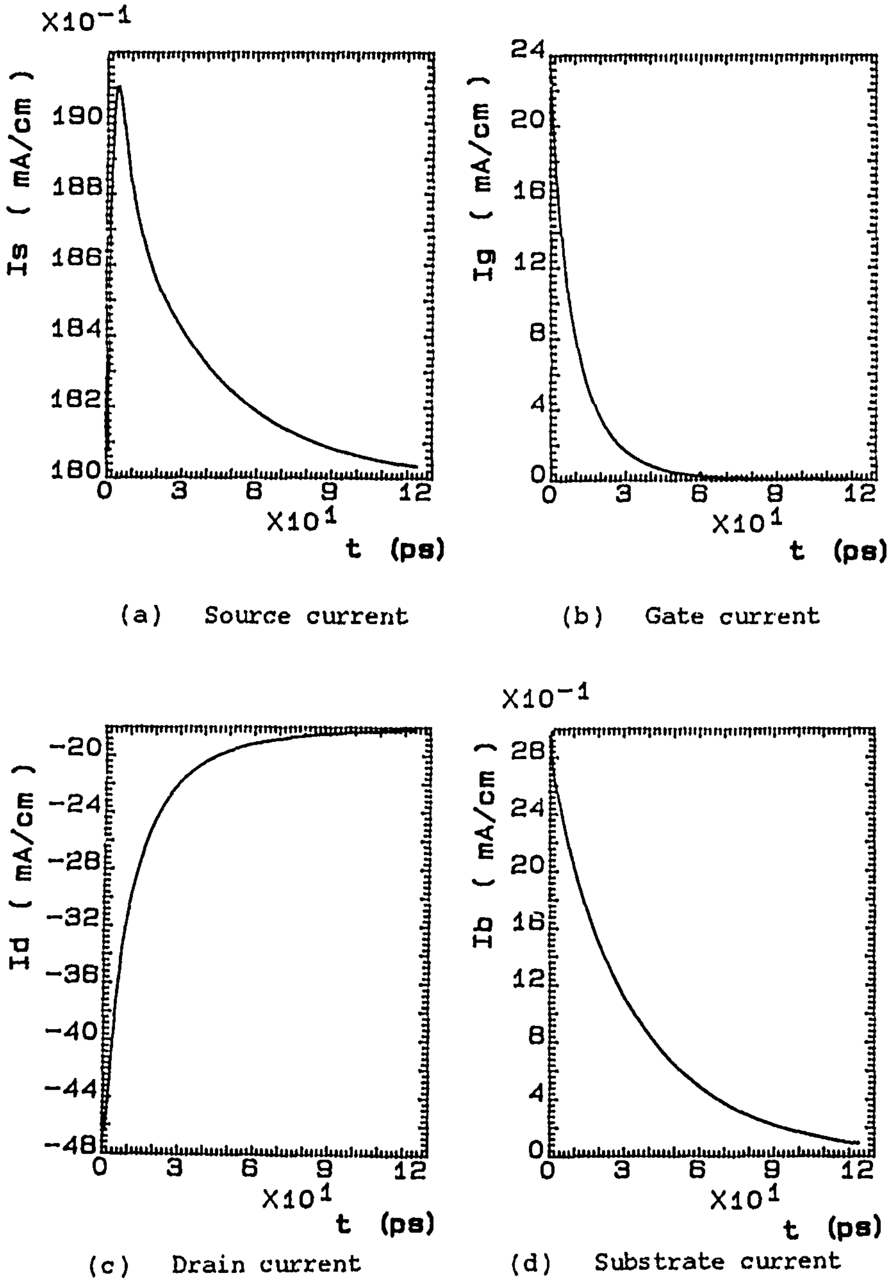


Fig. 8 Contact current transients of the recessed nMOS device for a step change in drain voltage from Vds=0.25V to Vds=0.5V

Fig. 7 presents the transient response of the recessed device at $V_{gs} = -1V$ to a step in drain bias from 0.25V to 0.5V. The source current remains almost constant throughout. The drain current starts at a very high value and then gradually decreases over the next 40ps. The high current corresponds to the removal of electrons from the drain end of the channel due to the effect of increased drain electric field on the inversion layer. The form of the gate displacement current, caused by the redistribution of potential within the channel, is similar but opposite in sign. The corresponding results for the planar device are given in fig. 8. Once again, they are similar in form to those of fig. 7, the main difference being the speed of switching.

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