

TWO/THREE-DIMENSIONAL DEVICE SIMULATOR

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ABSTRACT

We have developed a user-friendly versatile two/three-dimensional device simulator (ODESA).

With increasing device integration density in VLSI's, various parasitic effects such as fringe effects of wiring capacitance and latchup phenomena of CMOS structure are becoming more important factors, which are no longer negligible in designing VLSI circuits and devices. Analytical estimation of the parasitic effects is so difficult that device simulation has been essential for device and circuit designers. To accurately simulate various parasitic effects in VLSI devices by various designers, some simulation facilities such as three-dimensional or transient simulation have been required for device simulators.

We have first discussed versatility in a device simulator, and have recently extended the facilities of ODESA for three-dimensional potential analysis and two-dimensional transient analysis. And we will show two examples of simulation to estimate the efficiency of the extended facilities of ODESA.

1. INTRODUCTION

Device simulators have been developed for analyzing mainly MOSFET's [1]-[3] and have been a powerful design tool for developing VLSI devices.

With increasing device integration density in VLSI's, various parasitic effects such as latchup effects of CMOS structure, three-dimensional fringe effects of wiring capacitance and short/narrow channel effects of MOSFET's are becoming noticeable for designing VLSI circuits. And it has been difficult to develop VLSI's without accurately estimating the parasitic effects. As the analytical estimation has been difficult due to the two/three-dimensional problems, device simulators which can numerically calculate not only the electric

characteristics of MOSFET's but also the above parasitic effects are expected to be available for device and circuit designers. Since device simulators will be increasingly required to analyze any device structure for any purpose of analysis, we think device simulators should be developed taking versatility into account.

We have already developed a versatile two-dimensional device simulator and have estimated the algorithms for n-ch. MOSFET [4]. And we have recently extended the facilities of ODESA for three-dimensional potential analysis and two-dimensional transient analysis in order to analyze two typical problems in designing VLSI's.

In this paper, we first discuss versatility in a device simulator, and present construction of ODESA to realize the versatility and the algorithms concerning especially the recently extended facilities in ODESA. Finally, two examples of simulation for estimating the extended facilities of ODESA are presented, which are the results of three-dimensional wiring capacitance simulation and two-dimensional CMOS latchup analysis by transient simulation.

2. VERSATILITY OF DEVICE SIMULATION

Device simulation means to numerically solve the three fundamental partial differential equations of Poisson's equation and current continuity equations for holes and electrons under the given device configuration and the given boundary conditions. Simultaneously solving the equations generally requires much computation time and computer memory. And, with reducing device geometrical dimensions, various parasitic effects such as three-dimensional fringe effect of wiring capacitance or latchup phenomena of CMOS structure have been recently noticeable in designing VLSI's. Device simulators will be required to analyze such effects in arbitrary device configuration in a practical computation time. Therefore, we discuss versatility in a device simulation in this section.

1) User-friendly man-machine interface

Device simulation input data description generally becomes complicated in proportion to complexity of the device structure such as LDD-MOSFET and CMOS structure. Therefore, users have felt difficulty in accurately describing the input data for device simulators.

Since device simulators are, hereafter, expected to be used frequently for device and circuit designers to overcome various typical problems in designing VLSI's such as estimation of three-dimensional fringe effect of wiring capacitance or latchup effect of CMOS structure, man-machine interface such as user-friendly input data description language should be taken into account for developing device simulators.

2) Independence of device structure and dimension

Versatile device simulators must be able to analyze any device which is composed of arbitrary device configurations, device materials and arbitrary number of electrodes. This also means the device simulators to analyze not only two-dimensional device structure but three-dimensional device structure, if necessary.

3) A simulation execution sequence is automatically optimizable.

For numerically calculating device characteristics such as device internal behaviour or electrode current, the three-fundamental equations of Poisson's equation and current continuity equations for holes and electrons must be solved. But simultaneously solving the three equations is generally time consuming, still more the current continuity equations, for instance, are unnecessary to be solved in wiring capacitance simulation in which the entire device materials are generally composed of insulators and electrodes.

To obtain simulation results in a practical computation time, device simulators should be executed on previously selected equations with adequate physical models, considering the purpose of analysis.

4) Interface between device simulators and graphics systems, process simulators

Visually displaying simulation results by graphics systems is extremely effective to understand device internal behaviours such as carrier distribution of electrons and holes, electric field distribution. So, device simulators should be combined with graphics systems having good interface to realize versatility in device simulators.

In case of concerning linkage of process simulators with device simulators, device simulators must be able to distribute impurity profiles into the device simulation space. The impurity profiles are given by one-dimensional or two/three-dimensional process simulators. Therefore, the interface between device simulators and process simulators should be designed so as to select arbitrary combination of two simulators.

3. CONSTRUCTION OF ODESA

We discussed versatility in a device simulator in the previous section.

For implementing the versatility into our device simulator, we designed ODESA (Oki Device Simulation Art) as shown in Fig. 1. The versatile device simulator ODESA is divided into two parts of a main processor (DSS) and a pre-processor (PPDS).

DSS is a main processor of ODESA independent of device structure and discretizes a simulation space only using node information. (Detail algorithms of DSS are described in the next section.)

PPDS interprets user's input data file in which geometrical device configurations and the way of impurity mapping using one-dimensional process simulation results are described [5]. And PPDS, then, generates numerical input data file for DSS, which defines node attribution (NC) on discretized every node, boundary tables and also designs a sequence of simulation execution describing solved equations, physical models and accuracy of analysis.

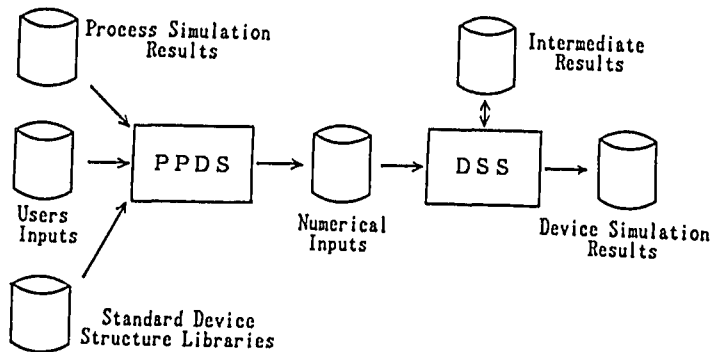


Fig. 1 Construction of ODESA (Oki Device Simulation Art)

Further we should like to add that device structure definition data of frequently used devices such as MOSFET's, CMOS's etc., are kept as default values in standard device structure libraries. Therefore, when the device in the libraries is used, simulation users have only to describe some parameters modified. And we have developed so user-friendly simulation input data description language (UNICOL) that difficulty of correct description on users' input data has extremely reduced. Figure 2. shows two examples of input data for three-dimensional wiring capacitance simulation and two-dimensional CMOS latchup simulation by transient mode. (The simulation results for the two input data will be presented in section 5.)

4. ALGORITHMS EXTENDED IN ODESA

We have already developed two-dimensional versatile device simulator [4] and have estimated its algorithms for n-ch. MOSFET. And we have recently extended the facilities of ODESA for three-dimensional analysis of Poisson's equation and two-dimensional transient analysis of current continuity equations for holes and

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*ODESA
  DEVICE=CAPACITOR, DIMENSION=3
*MODIFY
  X1   = 50.0
  X2   = 5.0
  X3   = 50.0
  X5   = 5.0
  X6   = 2.0
  X7   = 0.01
  X8   = 1.0
  X9   = 0.01
  X10  = 2.0
  X11  = 5.0
  DNX3 = 8, DRX3 = 0.625
  DNX4 = 3, DRX4 = 1.0
  DNY1 = 4, DRY1 = 1.0
  DNY4 = 7, DRY4 = 1.6
  DNY5 = 7, DRY5 = 0.625
  DNZ3 = 7, DRZ7 = 1.0
*RUN
  OUTP.POTENTIAL=MDL
  OUTP.FIELD=ML
  V1=0.0, V2=5.0, V3=0.0, V4=0.0
*END

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(A)

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*ODESA
  DEVICE=CMOS, DIMENSION=2
*MODIFY
  CAR=TWO, RCB=AUGER, TRANSIENT=Y
  X3   = 10.0
  X4   = 30.0
  X5   = 4.0
  X6   = 10.0
  SBD  = 40.0
  DNX4 = 4, DRX4 = 1.25
  DNX6 = 4, DRX6 = 0.8
  DNX9 = 3, DRX9 = 1.0
  DNX3 = 6, DRY3 = 1.25
  DNY4 = 6, DRY4 = 0.8
*RUN
  OUTP.POTENTIAL=M
  OUTP.ELECTRON=DM
  OUTP.HOLE=DM
  FI=0
  V1=5.0, V2=5.0, V3=0.0, V4=0.0
*RUN
  MD=TR, FI=IO, IN=RC
  V1=5.0, V2=5.0, V3=0.0, V4=0.2, TIME=2E-11
*END

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(B)

Fig. 2 Two examples of input data for (A) the three-dimensional wiring capacitance simulation and (B) the two-dimensional CMOS latchup simulation by transient mode

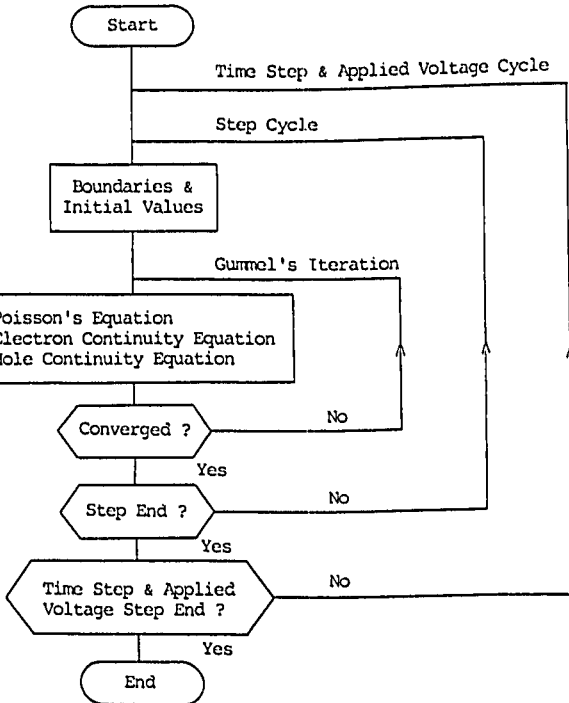


Fig. 3 Flow-chart of ODESA

electrons. We show the algorithms concerning mainly the extended facilities of ODESA.

4.1 FLOW-CHART OF DSS

A flow-chart of DSS is shown in Fig. 3. There consists three do-loops. The inner loop is Gummel's iteration loop [6] alternatively solved the fundamental equations of Poisson's equation and the current continuity equations for holes and electrons.

The outer loop is time step and applied voltage cycle iterating every bias condition and every time step in transient simulation. That is, applied voltage are assumed to change with advancing time steps in transient simulation.

The intermediate do-loop is called "step cycle" [4]. In each step cycle, solved equations, physical models and accuracy of analysis are indicated by the numerical input file shown in Fig. 1. Generally, with advancing the step, grading the solved equations up. That is, the step cycle enables the effective and optimized execution to realize in a device simulator.

4.2 DISCRETIZATION ALGORITHMS IN DSS

DSS performs device simulation independent of device structures and user's requirements, according to the designed steps and the information about nodes and boundaries.

In each step of device simulation, the Poisson's equation and current continuity equations for holes and electrons are solved.

The continuous forms of the equations in semiconductor are

$$\nabla \cdot (\epsilon \nabla \psi) = -q(p - n + \Gamma) - Q_{ss} \quad (1)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} \text{div} J_n + (G - R) \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \text{div} J_p + (G - R) \quad (3)$$

where

$$J_n = q(D_n \nabla n - \mu_n n \nabla \psi) \quad (4)$$

$$J_p = -q(D_p \nabla p + \mu_p p \nabla \psi) \quad (5)$$

Here, ψ , Γ and Q_{ss} are electrostatic potential, impurity concentration and charge concentration representing the fixed charge at the silicon/silicon dioxide interface. n and p are the electron and the hole concentrations. J_n and J_p are the electron and hole current densities, G and R are the generation and recombination rates, μ_n and μ_p are the electron and hole mobilities, D_n and D_p are the electron and hole diffusivities,

and q are the permittivity and the absolute value of an electron charge. In insulator, n , p and r are assumed to be zero value.

1) Poisson's equation

In DSS, the Poisson's equation (Eq.(1)) is linearized by Gummel's algorithm [6], and expressed as

$$\nabla \cdot (\epsilon \nabla \delta) - \frac{q^2}{kT} (n+p) \delta = -\nabla \cdot (\epsilon \nabla \psi^{(m)}) - q(p-n+\Gamma) - Q_{ss} \quad (6)$$

where

$$\delta \equiv \psi^{(m+1)} - \psi^{(m)}$$

Here, k , T and m are Boltzmann constant, temperature and iteration number, respectively.

Finite difference method with the box integration method is applied to Eq. (6). DSS permits arbitrary boundary such as semiconductor/insulator interface boundaries and external Neumann-type boundaries transversing through the cuboidal cell.

Figure 4. shows a cuboidal cell exclusively shared by a node in three-dimensional orthogonal grid system. The cell is surrounded by six planes perpendicularly bisecting each branch which connects the center node and the adjacent node, and is composed of fourty eight sub-cells. Each sub-cell is a right-angled triangular prism which base composes a piece of surface area of the cuboidal cell and height is defined as a distance between the base and the center node. Then, the discretized equation is expressed as follows;

$$\begin{aligned} & \sum_{i=1}^6 \sum_{j=1}^8 \frac{\epsilon_{ij}}{q} \cdot \frac{\delta_i - \delta_0}{h_i} \cdot s_{ij} - \frac{q}{kT} (n+p) V \delta_0 \\ & = - \sum_{i=1}^6 \sum_{j=1}^8 \frac{\epsilon_{ij}}{q} \cdot \frac{\psi_i - \psi_0}{h_i} \cdot s_{ij} + (n-p-\Gamma) V - Q_{ss} S \end{aligned} \quad (7)$$

where ϵ_{ij} and s_{ij} are permittivity and base area of the sub-cell, and h_i is a distance between the center node and the adjacent node. V is a volume of the cuboidal cell shared by semiconductor materials, S is an area of cross-section of semiconductor/insulator interface transversing through the cuboidal cell. The third term of the right-hand side in Eq.(7) is considered if the node attribution (NC) of the center node is an "interface".

2) Current continuity equations

In DSS, the current continuity equations (Eq.(2) and (3)) once integrated by Green's theorem is discretized by Scharfetter-Gummel's algorithm [7], and is applied for two/three-dimension. And time-dependent term is approximated by difference of the first order, and is applied only for two-dimensional simulation. Two-dimensional discretized current continuity equations are generally expressed as follows;

equation degenerated from Poisson's equation. The two strip lines of wiring crossing each other, ERD.1 and ERD.2 with a cross-section of $1 \times 1 \text{ } \mu\text{m}^2$, respectively, are separated by $1 \text{ } \mu\text{m}$ from their intersection. The interface between the silicon-dioxide and the air is assumed to be $1 \text{ } \mu\text{m}$ upward from ERD.1. ERD.3 is assumed to be ground-biased as a surface of semiconductor bulk.

The three-dimensional capacitance value between ERD.1 and ERD.2 in Fig.6-1(a) is $2.16 \times 10^{-4} \text{ pF}$, and the analytical value assumed parallel planes is $3.45 \times 10^{-5} \text{ pF}$. The result shows that we can evaluate fringe capacitance, which shares more than 80 % of the three-dimensional wiring capacitance and is no longer negligible in designing VLSI circuits.

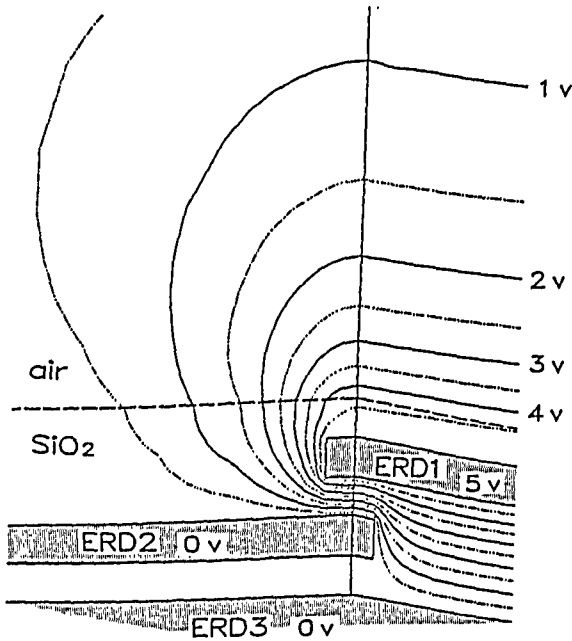


Fig. 6-1(a) Equipotential lines by three-dimensional wiring capacitance simulation

Figure 6-1(b) shows electrode width dependence of three-dimensional wiring capacitance. C , W , T and H are the wiring capacitance between the two strip lines, electrode width, electrode thickness and distance between the two strip lines, respectively. With decreasing the W , the C decreases nearly quadratically when the H is comparatively negligible to the W . However, the C does not remarkably decrease when the dimension of the W becomes nearly equal to and smaller than the H . The result is caused by fringe effect between the two strip lines.

With reducing device and wiring dimensions, sensitivity to

fringe capacitance between two strip lines three-dimensionally crossing each other can not be accurately analyzed by two-dimensional simulation because of the three-dimensional effect. We find that ODESA is extremely useful to evaluate fringe capacitance of two wirings in designing VLSI circuits.

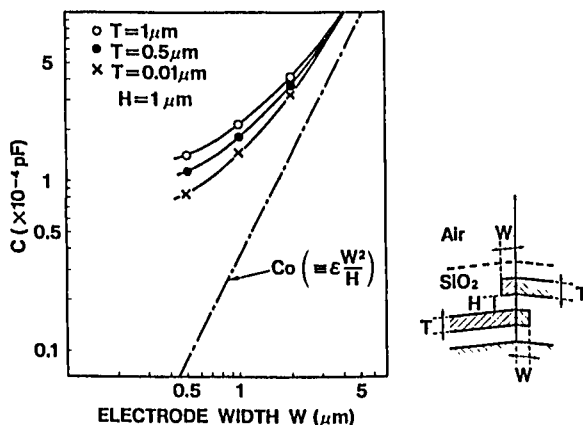


Fig. 6-1(b) Electrode width dependence of the wiring capacitance of two strip lines crossing each other in three-dimensional simulation

2) Transient simulation of CMOS latchup

To estimate another extended facility of ODESA, latchup simulation of CMOS structure shown in Fig.6-2(a) by two-dimensional transient mode is presented. $\xi=0$ is taken as a transient parameter.

In the figure, V2 and V3 are source/drain contacts of p-ch. and n-ch. MOSFETs, respectively. V1 is located on the surface to accurately consider the substrate resistance which is sensitive for CMOS latchup phenomena. The external boundaries in the substrate bulk are assumed to be Neumann-type boundary.

An external trigger voltage 0.97/0.1ns is applied to V4 with 5v reversely-biased across the p-well junction.

We see that at $t=1\text{ns}$ the electrons injected from n+ diffusion layer have reached to the n- substrate collector of the parasitic vertical npn transistor, as shown in Fig.6-2(b). With increasing electrons in the n- substrate as a collector current of vertical npn transistor, holes in the p+ diffusion layer also come to flow into the n- substrate due to maintaining equilibrium state, as shown in Fig.6-2(c) ($t=8\text{ns}$). Some of the holes flow into the p-well as a collector current of the parasitic lateral pnp transistor. They also promote electrons to inject from n+ diffusion layer. Figure 6-2(d) shows direction of hole current density at $t=8\text{ns}$, which means the beginning of CMOS latchup

action.

We find that ODESA is effective for transient analysis such as CMOS latchup phenomena in VLSI devices.

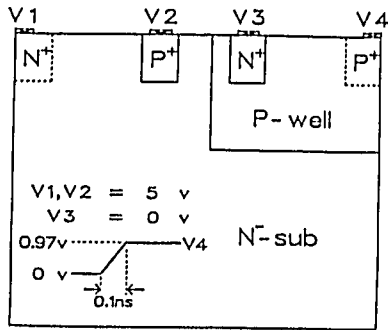


Fig. 6-2(a) Device structure for two-dimensional transient simulation of CMOS latchup

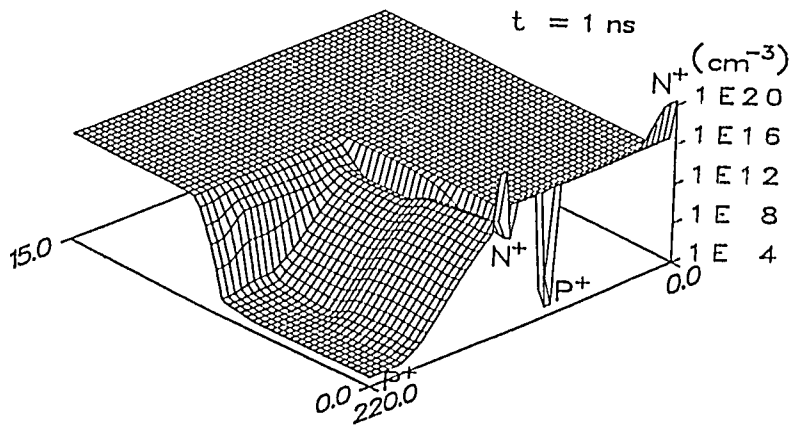


Fig. 6-2(b) Log plot of electron concentration

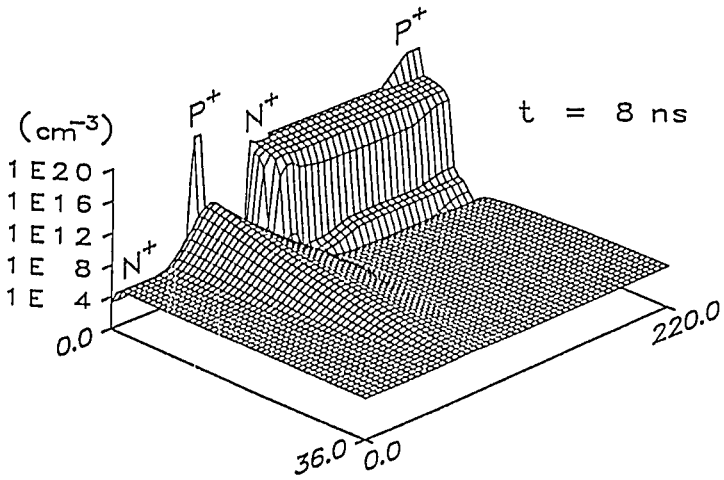


Fig. 6-2(c) Log plot of hole concentration

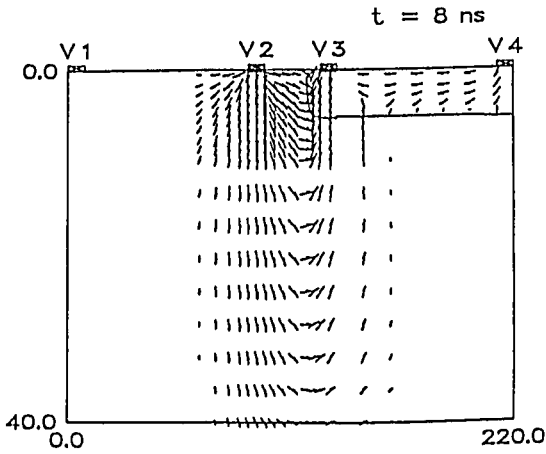


Fig. 6-2(d) Direction of hole current density which shows the device turns on

6. CONCLUSION

With increasing device integration density, various parasitic effects to be estimated have been so remarkable that device simulators which can analyze arbitrary device structure for any purpose of simulation have been increasingly essential for designing VLSI's.

Most of the design philosophies of the versatility have been already reflected in the two-dimensional device simulator (ODESA) in which the implemented algorithms were estimated for n-ch. MOSFET.

Focusing on some current topics on device and circuit designing, we have extended the facilities of ODESA for three-dimensional potential analysis and two-dimensional transient analysis which are considered as a part of versatility in device simulators. And, we have developed versatile two/three-dimensional device simulator.

To estimate the extended facilities of ODESA, two examples of simulation (i.e. three-dimensional wiring capacitance simulation and two-dimensional CMOS latchup simulation by transient mode) were shown. We find that the facility of three-dimensional potential analysis is effective for estimating the three-dimensional fringe effect of wiring capacitance, and that another facility of two-dimensional transient simulation is also effective to understand the device internal behaviours changing with advancing time step.

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