TOWARDS A PHYSICAL MODEL OF CARRIER MOBILITY FOR DEVICE SIMULATION

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1 ABSTRACT

This paper critically discusses the semi-empirical expressions currently used to model carrier mobility in device-simulation codes. In particular, the physical principles underlying the mobility degradation mechanisms are examined. Experimental data is presented for the dependence of inversion layer mobility in n- and p-channel MOS devices on temperature, ionised impurity concentration, confining (vertical) electric field and drift (horizontal) electric field. Results of a theoretical study of the population of 2D energy levels in n-channel inversion layers as a function of temperature and confining electric field are presented.

It is concluded that the different physical environments experienced by carriers in inversion layers compared with carriers in bulk silicon make it desirable to use separate mobility models for the two regions.

2 INTRODUCTION

Any quantitative analysis of device operation based on the drift-diffusion and current continuity equations relies heavily on accurate models for the physical parameters (i.e. mobility, diffusivity and the generation-recombination-rates) appearing in these equations.

The mobility parameter is of particular importance for two reasons; because of the multiplicative dependence of the currents on it and because under appropriate physical conditions the diffusivity may be directly obtained from it using the Einstein Relation.

This paper discusses the semi-empirical expressions commonly used to model carrier mobilities, and presents new experimental data. Particular attention is paid to inversion layer mobilities. The major mobility controlling parameters considered are vertical electric field, temperature, ionised impurities and velocity saturation.

3 MOBILITY IN BULK SILICON

There are two major controlling parameters to be considered when modelling mobility in bulk silicon; temperature and ionised impurity concentration. For lightly doped samples the mobility temperature dependence may be associated with lattice scattering and is typically modelled over the temperature range $250K < T < 400K$ using a power law expression

$$\mu_L = \mu_0 (T/300)^{-\alpha_L} \qquad (1)$$

where μ_L denotes the 'lattice mobility'.

Physically based theoretical expressions for ionised impurity scattering also exist in the literature [1]. One approach to obtaining a combined temperature and ionised impurity dependent mobility is to combine the expression found in [1] with equation (1) using the appropriate combining function.

From a device modelling viewpoint, this approach has two serious drawbacks

(i) The expression used to combine lattice and ionised impurity mobilities is a complicated one [2]. This can lead to an inefficient implementation of the model in a device simulation code.

(ii) Physically based theoretical expressions for ionised impurity scattering such as that found in [1] have a limited range of validity. At high doping levels where the effects of multiple scattering become important and different mobilities are reported for different dopant species there is a lack of models which accurately describe the experimental data. Doping levels of order 10^{20} cm^{-3} are potentially of interest from a device simulation viewpoint, both in the source/drain regions of an MOS device, where an accurate value of mobility is required for series resistance calculations and in the emitter region of a bipolar device. Thus one is forced to consider empirical expressions for the combined lattice and ionised impurity mobilities.

In this study, we have used the Caughey/Thomas expression [3] plus the corrections suggested by Massetti et al. [4] at high doping concentrations. These are detailed below.

The Caughey/Thomas expression reads

$$\mu^{LI} = \mu_{min} + \frac{\mu^{L} - \mu_{min}}{1 + \left[\frac{CI}{C_r}\right]^{\alpha}} \qquad (2)$$

where

$$CI = \sum_{i=1}^{N} |Z_i| N_i \qquad (3)$$

is the sum of the concentrations of the ionised species multiplied by the magnitude of their charge and μ^{L} is given by (1).

Above 5×10^{18} cm^{-3} deviations from equation (2) are expected, in particular we note that in the limit $CI \to \infty$ then equation (1) predicts $\mu^{LI} \to \mu_{min}$ which is physically unreasonable.

Masetti et al. [4] have investigated the mobility of As, B and phosphorus doped silicon. By using laser annealing they have investigated active doping concentrations in excess of the solid solubility limits. The expressions found are quoted below. These are valid for P, and As active concentrations up to 5.0×10^{21} and B up to 1.2×10^{21} cm^{-3}.

For Arsenic and Phosphorus:

$$\mu^{LI} = \mu_{min} + \frac{\mu^{L} - \mu_{min}}{1 + (CI/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/CI)^{\beta}} \qquad (4)$$

and for Boron:

$$\mu^{LI} = \mu_{min} \exp\{C_t/CI\} + \frac{\mu_L}{1 + (CI/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/CI)^{\beta}} \qquad (5)$$

The values of the various parameters used in equations (2),(4) and (5) are quoted in Table 1.

Temperature dependences have also been suggested for parameters other than μ_L in equations (2)-(5) [5].

Table 1

Lattice/impurity mobility model parameters

	Arsenic	Phosphorus	Boron	Units
μ_{min}	52.2	68.5	44.9	$cm^2\ V^{-1}\ s^{-1}$
μ_L	$1416\ (T/300)^{-2.33}$	$1416\ (T/300)^{-2.33}$	$470.0\ (T/300)^{-2.23}$	$cm^2\ V^{-1}\ s^{-1}$
μ_1	43.4	56.1	29.0	$cm^2\ V^{-1}\ s^{-1}$
C_r	9.69×10^{16}	9.20×10^{16}	2.23×10^{17}	cm^{-3}
C_s	3.43×10^{20}	3.41×10^{20}	6.10×10^{20}	cm^{-3}
α	0.680	0.711	0.719	
β	2.00	1.98	2.00	
C_t	--	--	9.23×10^{16}	cm^{-3}

4 MOBILITY AT SURFACES

The state of knowledge of carrier mobility in surface inversion layers is far less advanced than for bulk silicon. Certainly one does not expect that the ionised impurity mobility expression and parameters such as the lattice temperature exponent and velocity saturation co-efficients to be the same as in bulk silicon due to the different energy level structure experienced by carriers in inversion layers [6]. Detailed studies using the method outlined in ref [6] have revealed that at room temperature only a handful of two dimensional energy levels are occupied for typical inversion layer fields for both electrons and holes.

Figure 1 shows a plot of inversion layer energy level population at room temperature for electrons. In this case the confining potential $\phi(z)$ has been approximated by a triangular potential well, and Boltzmann statistics for the electrons have been assumed.

This leads one to believe that a classical treatment of inversion layer transport where the effect of surface confinement is treated by an empirical surface roughness expression may be inaccurate. The authors have developed a mobility model which treats the surface transport and bulk regimes separately. This allows the possibility to include different temperature dependences, impurity scattering and velocity saturation co-efficients for the two regimes.

4.1 p-channel experimental data; doping variation

p-channel devices were fabricated on 5 μm 7 Ωcm n-type epitaxial substrates on the (100) orientated Si surface. Subsequently boron and phosphorus channel implants were used to increase the surface ionised impurity concentration whilst

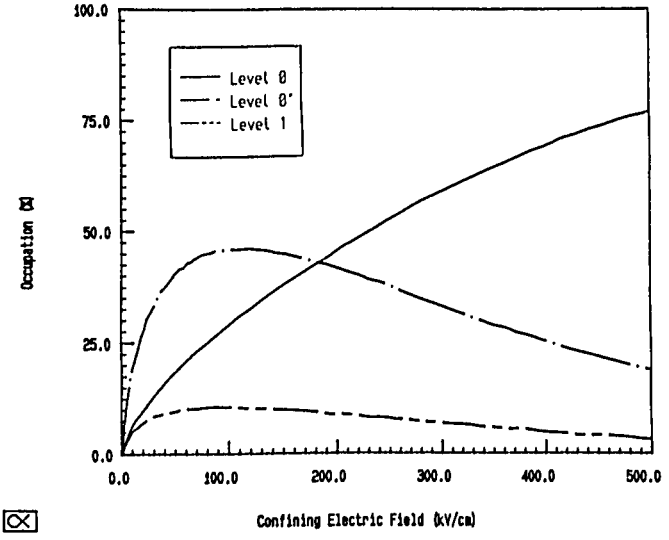

Figure 1 : Lowest lying electron energy level occupations vs vertical electric field for the (100) orientated silicon surface at 300 K.

maintaining a roughly constant threshold voltage. The implants used together with the modelled net doping concentrations obtained from SUPREM II are outlined in Table 2.

Table 2

p-channel devices : simulated doping concentratons

Split	Boron	Phosphorus	Simulated Surface Dopant Conc.		
	@25 keV	@180 keV	B cm^{-3}	P cm^{-3}	$N_D^+ + N_A^-$ cm^{-3}
1	0 cm^{-2}	0	-	7.0E14	7.0E14
2	4E11	4E11	2.4E16	4.0E15	2.8E16
3	6E11	6E11	3.5E16	5.5E15	4.1E16
4	7E11	8E11	4.1E16	7.0E15	4.8E16
5	8E11	10E11	4.7E16	8.5E15	5.6E16
6	9E11	12E11	5.3E16	1.0E16	6.3E16

For all splits the channel implants received a total of 87 mins heat treatment at 950°C. The hole mobility is plotted against average inversion layer electric field [7] in Figure 2 for splits 1,3,5, and 6. Also plotted are the best fits to each set of data using equation (6).

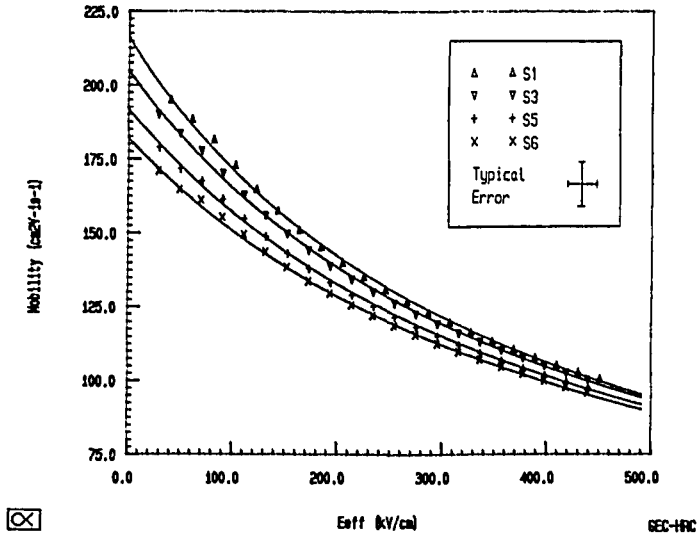

Figure 2 : Hole mobility vs effective vertical electric field for p-channel inversion layers with total ionised doping concentrations as indicated in Table 2.

$$\mu = \frac{\mu_0}{1 + \theta E_y} \qquad (6)$$

The results indicate a clear reduction in carrier mobility at low electric fields for ionised impurity concentrations of the order $2 \sim 6 \times 10^{16}$ cm^{-3}.

The temperature dependence of the mobility at threshold has been investigated for splits 1 and 6 (Figure 3). For split 1 the total ionised dopant concentration is sufficiently low that the temperature dependence obtained may be associated with the term μ_L in equation (1). One finds a significantly different temperature exponent for inversion layers compared with the bulk regime (c.f. Table 1). The reduction in temperature exponent found for split 6 suggests that the mobility reduction mechanism associated with splits 1 to 6 has a temperature exponent greater than -1.62. This is consistent with impurity scattering.

4.2 n- and p-channel experimental data: vertical field dependence

Sabnis and Clemens [7], showed that the dependence of inversion layer mobility on gate bias, back bias and channel doping (at low concentrations where ionised impurity scattering can be neglected) could be described using a single parameter, the effective electric field normal to the interface.

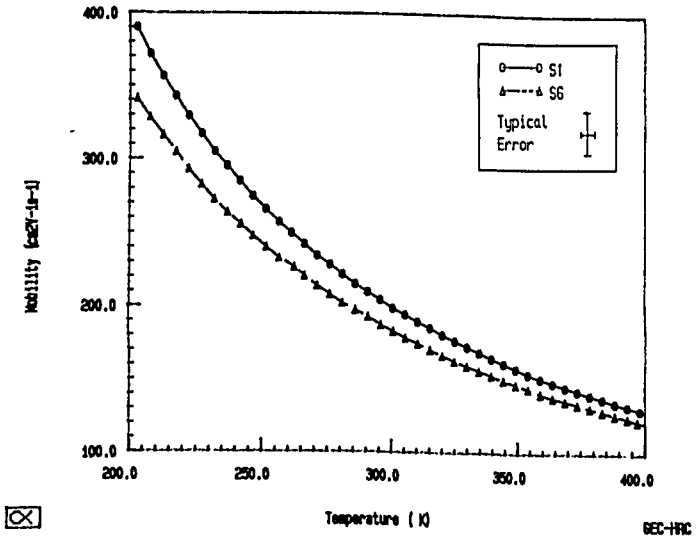

Figure 3 : p-channel inversion layer mobility at threshold vs temperature. The power law dependences on temperature obtained were : split 1 $\mu = \mu_0(T/300)^{-1.62}$, split 6 $\mu = \mu_0(T/300)^{-1.52}$.

$$E_{eff} = \frac{1}{\varepsilon_0 \varepsilon_{Si}} (Q_B + Q_N/2) \qquad (7)$$

In their case, the devices measured were n-channel (100) orientated and fabricated on p-type 4-5 Ωcm bulk material. Several implant doses from 0 to $2x10^{12}$ boron and compensating 0 to $2x10^{12}$ cm^{-2} phosphorus were used to increase the surface layer doping.

In this work the effects of substrate bias, gate bias and channel doping on both n- and p-channel devices have been investigated. The processing conditions investigated are outlined in Table 3.

Figure 4 shows the n-channel inversion layer mobility plotted against the effective electric vertical field for batches N1 and N2. In the case of batch N2 the variation of mobility with vertical electric field as the substrate bias is varied is also shown.

Figure 5 shows the p-channel inversion layer mobility plotted against the effective vertical electric field for batch P1. The vertical electric field is obtained from equation (7) where Q_B is obtained from a 1D Poisson's equation solution given the doping profile supplied by a SUPREM II simulation of the relevant batch processing conditions.

Table 3

Processing conditions for batches N1,2 and P1

Batch	Starting material (p-well doping)	Channel Implants Boron @25 keV	Channel Implants Phosphorus @200 keV	Interface doping (SUPREM II) $N_D^+ + N_A^-$	Oxide thickness
N1	($8.0x10^{15}$)	3E11	3E11	$2.8x10^{16}$	400 Å
N2	($8.0x10^{15}$)	-	-	$6.9x10^{15}$	400 Å
P1	20-30 Ω cm Bulk n-type	2.5E11	1E11	$1.6x10^{16}$	400 Å

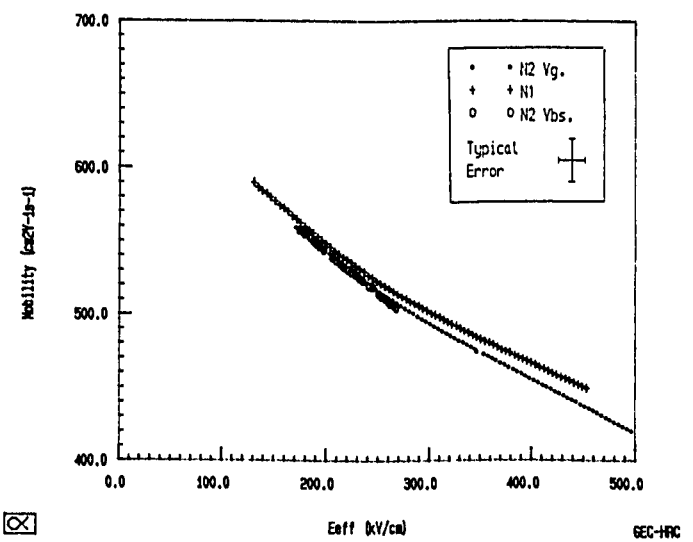

Figure 4 : Electron mobility vs effective vertical field for batches N1 and N2 showing the effect of varying substrate bias and gate bias.

Our results are consistent with the conclusion of Sabnis and Clemens [7]; that the variation of mobility with effective field can be described by a single curve with both gate and substrate biases applied. It should be noted however that the p-channel batch presented shows a poor substrate sensitivity due to its low background doping. This has allowed us to look only over a small variation of vertical field with back bias.

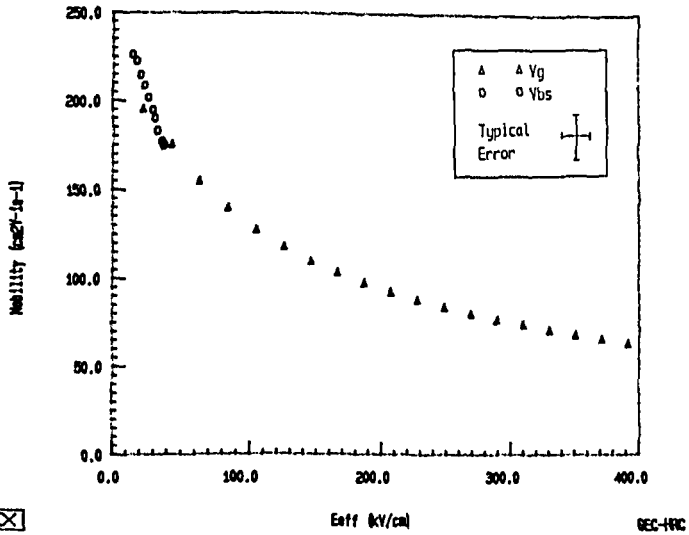

Figure 5 : Hole mobility vs effective vertical field for batch P1 showing the effect of varying substrate bias and gate bias.

When seeking a mobility model for use in device simulation, it is important that the range of applicability of that model is known. So far we have suggested that our low drift electric field measurements of surface mobility from two batches of wafers can be explained by a model including the effects of vertical field and lattice scattering whilst ionised impurity scattering only starts to be important at concentrations above 10^{16} cm^{-3}. To see if the model we have derived can be applied to devices made by different processes using alternative starting material we have measured the mobility on devices made by two UK manufacturers of MOS devices and in Figure 6, compared these results together with the 'universal curve' of ref [5]; clearly this graph suggests that a universal mobility model cannot be generated unless further controlling parameters are identified, but to date it is unclear whether these parameters should relate to the starting material (epi-silicon quality), the interface roughness or the oxide charge. Therefore we recommend that, for accurate simulations, a mobility model must be calibrated to the process.

4.3 n- and p-channel experimental data: Velocity saturation effects

The velocity-drift electric field relationship for electrons in silicon inversion layers has been investigated by several workers. The problem of analysing high electric field data is complicated by the fact that the saturation of electron velocity leads to an inhomogeneous electric field

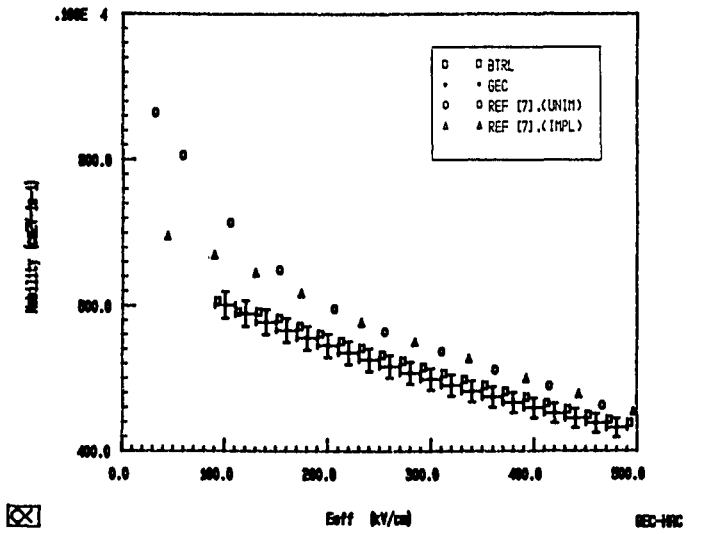

Figure 6 : Mobility vs vertical electric field plotted for devices supplied by BTRL compared with the 'universal curve' of ref [7] and devices supplied by GEC.

distribution along the channel. The problem has been addressed using many methods: resistive gates [8], time of flight measurements [9] and self consistent analysis [10]. The authors believe that the method is outlined in ref [10] is instructive and have developed the algorithm further.

Both n- and p-channel devices have been investigated over a temperature range from 200K to 400K. Figure 7 shows the velocity field curves obtained for an n-channel device with an electrical channel length of 0.99 μm at 300K with applied gate biases of 5V,10V,15V and 20V. The following preliminary comments can be made:-

(i) the reduced velocity as the gate bias increases for low horizontal fields is to be expected from the dependence of low field mobility on vertical field already reported

(ii) for any given gate bias condition one finds the carrier velocity decreases monotonically as the temperature is increased

(iii) the carrier velocities measured are not inconsistent with saturation velocities quoted elsewhere [11,12] at 1.1×10^7 cms^{-1} for electrons and 9.5×10^6 cms^{-1} for holes.

Further work is underway to include the effect of variation of vertical electric field along the channel into the analysis and to explore various empirical velocity-electric field fits to the data.

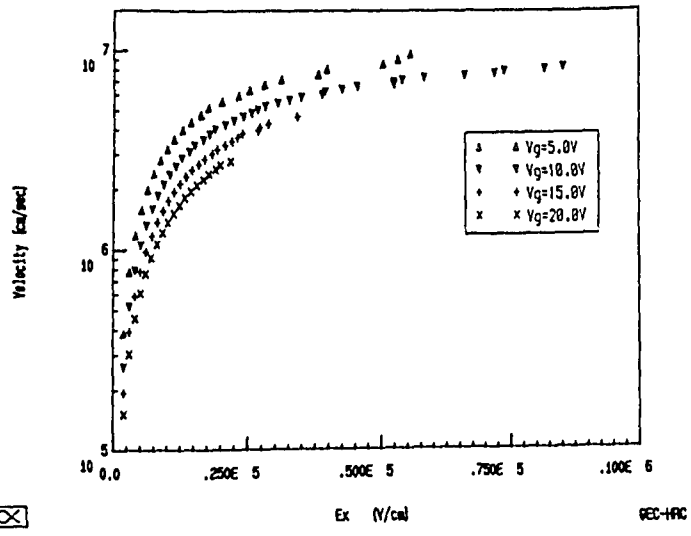

Figure 7 : Electron carrier velocity vs parallel electric field at 300 K for various gate bias conditions.

5 IMPLEMENTATION OF THE DEVICE SIMULATION MODEL

As a result of our experimental investigations a device simulation mobility model has been developed. This model has been successfully coded into MINIMOS and the device simulation code MADMACS developed at HRC. Figure 8 shows the agreement

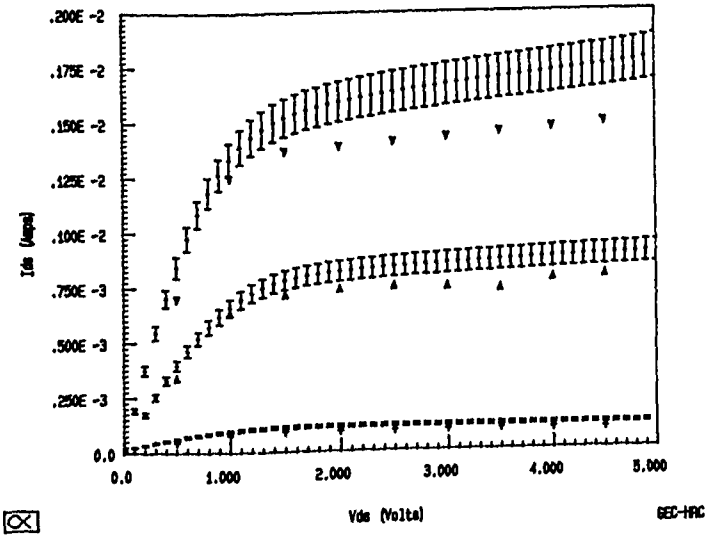

Figure 8 : Comparison of experiment I-V curves with simulated curves obtained using our mobility model. 3 channel length devices are shown: L=20 μm(+), 3 μm(Δ) and 1.5 μm(∇) with a gate bias of 3V at 22°C. The experimental points are denoted by error bars.

with experiment obtained using the mobility model for a series of n-channel MOS devices with channel lengths from 20 to 1.5 μm. The simulations were carried out using the MINIMOS code at a temperature of 22°C using the 2 dimensional unipolar model. Figure 9 shows a perspective plot of carrier mobility for the 5 μm p-channel device using this model.

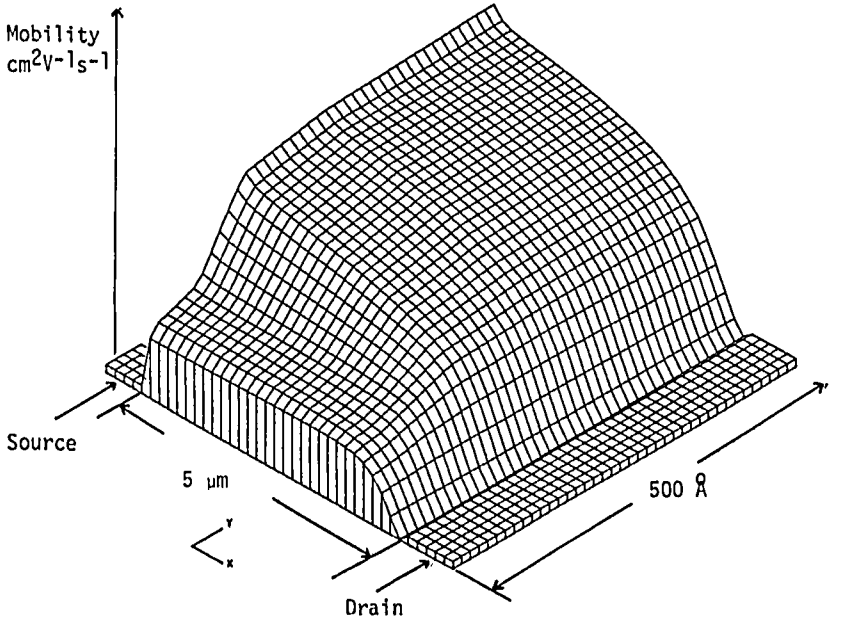

Figure 9 : 2 dimensional plot of carrier mobility for a 5 μm p-channel device using our mobility model.

It should be noted that the device modelling environment places additional constraints on the model developed. Derivatives of the mobility function are required if second order convergence of the non-linear Newton Scheme is to be guaranteed. We thus require expressions which are continuous and sufficiently simple so that derivatives can be efficiently extracted.

A particular problem with our model is the incorporation of smooth transition between 'surface' and 'bulk' regions of the MOS device. At present the electric field perpendicular to the interface is used as a parameter for this transition. Other ideas being explored are the use of the electric field perpendicular to the direction of current flow and the perpendicular distance from the interface.

6 CONCLUSIONS

We have highlighted some problem areas in the development of more accurate mobility models, as well as areas where a good measure of success has already been achieved in developing semi-empirical expressions, valid over a range of physical conditions.

Despite these problems, good quantitative agreement with experiment has been achieved by developing a model of carrier mobility using physically motivated expressions wherever possible. One accepts that with our current state of knowledge of mobility reduction mechanisms, particularly for surface transport, some of the parameters used in the model may be process dependent.

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