SIMULATION OF III-V DEVICES SEMI-INSULATING MATERIALS

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ABSTRACT : Semi-insulating materials are commonly used in III.V components. Semi-insulating doping density comes out the equilibrium of high density deep centers with the free carriers. The transport equation set is completed to describe the semi-insulating materials behavior. GaAs FET active layer on SI substrates and GaInAs active layer on InP SI substrate are presented. GaInAs/InP JFET is simulated.

1 - INTRODUCTION

Devices using III-V materials are often elaborated on semi-insulating substrates either for discrete components or integrated circuits. The semi-insulating material is used for its high resistivity characteristics and insulating properties.

Fied effect transistors have an n doped active layer which is either realized by epitaxy or direct implantation of the semi insulating substrate.

The FET's characteristics would mainly be related to the FET geometry if the semi insulating material had a perfect dielectric behaviour. This is often assumed. But it is also well known that a space charge region exists between the active layer and the semi insulating substrate. The space charge region extension depends on the component bias. Therefore the effective active layer thickness depends on the equilibrium between the active layer and the semi insulating material.

The first effect is to decrease the thickness of the active layer when increasing drain-source bias (Vds), which is a critical matter when considering the pinch off behaviour.

As far as integrated circuits are concerned, a second effect is related to the influence of neighbouring components bias, through the semi insulating material, on the equilibrium of a component. This effect is known as side-gating.

When simulating FET's the influence of the semi insulating material must not be neglected.

Now a days III-V FET's are either GaAs MESFET's on GaAs semi insulating material or GaInAs JFET's on InP semi insulating substrate. In both cases the SI materials are obtained by compensation of shallow residual impurities by one or a few deep levels in relatively high densities. The ionization of the deep centers results from the equilibrium with the free carriers densities and therefore depends on the applied bias. From a numerical point of view this means that the doping concentration is not a constant.

In previous papers (1,2)we have shown that the electrochemical and electrostatic potentials are a most adequate set of variables to describe heterostructures. This representation is well adapted to compute low substrate current for which accurate methods are needed. The impurity concentrations in the SI material are some $10^{15} - 10^{17}$ cm^{-3} whereas the carrier densities are as low as $10^{6} - 10^{8}$ cm^{-3}.

We shall describe the interface equilibrium either for an n GaAs on SI GaAs and for a GaInAs layer on SI InP, in one dimensional simulation and for a bidimensional FET simulation.

The transport equation set is summarized below.

2 - TRANSPORT EQUATION SET

The steady state transport equation set is :

$$\operatorname{div} \varepsilon \overrightarrow{\operatorname{grad}}\, \phi = q(n-p-C) \qquad (1)$$

$$\operatorname{div} n\mu_n \overrightarrow{\operatorname{grad}}\, \phi_n = -U \qquad (2)$$

$$\operatorname{div} p\mu_p \overrightarrow{\operatorname{grad}}\, \phi_p = U \qquad (3)$$

where $E_{fn} = - q\phi_n$ and $E_{fp} = - q\phi_p$ are the electrochemical potentials. C is the doping density which depends on the deep impurities ionisation in the case of largely compensated semiconductors such as semi insulating-materials. $C = \sum [N_D^+ - N_A^-]$ For a given center, depending on the type:

$$N_A^- = N_A \frac{C_n n + C_p p_1}{C_n(n+n_1) + C_p(p+p_1)} \qquad (4)$$

$$N_D^+ = N_D \frac{C_p p + C_n n_1}{C_n(n+n_1) + C_p(p+p_1)} \qquad (5)$$

where $C_n = \sigma_n v_n$ $\quad C_p = \sigma_p v_p$ $\quad \sigma_{n,p}$ the capture cross section $\quad v_{n,p}$ the thermal velocity

We have establish that in Fermi-Dirac statistics

$$n_1 = n \exp[(E_T - E_{fn})/kT] \ , \ p_1 = p \exp[(E_{fp} - E_T)/kT] \qquad (6)$$

where E_T is the energy level of the center in the band gap.

In the Maxwell-Boltzmann approximation it becomes:

$$n_1 = N_c \exp[-\Delta E_T/kT] \ , \ p_1 = N_v \exp[(-E_g + \Delta E_T)/kT] \quad \Delta E_T = E_c - E_T$$

To solve the non linear Poisson equation, it is necessary to define the following differential quantities.

$$D = \{ C_n(n+n_1) + C_p(p+p_1) \}$$

$$\frac{\partial N_A^-}{\partial \phi} = N_A \{ (C_n n_1 + C_p p) C_n \frac{\partial n}{\partial \phi} - (C_n n + C_p p_1) C_p \frac{\partial p}{\partial \phi} \} / D \qquad (7)$$

$$\frac{\partial N_D^+}{\partial \phi} = N_D \{ (C_p p_1 + C_n n) C_p \frac{\partial p}{\partial \phi} - (C_p p + C_n n_1) C_n \frac{\partial n}{\partial \phi} \} / D \qquad (8)$$

$$\frac{\partial C}{\partial \phi} = \sum \left(\frac{\partial N_D^+}{\partial \phi} - \frac{\partial N_A^-}{\partial \phi} \right)$$

By writing $\phi = \phi_o + \delta\phi$, ϕ_o Poisson equation can be written in the following way :

$$\text{div } \varepsilon \vec{\text{grad}}\, \delta\phi - q\left(\frac{\partial n}{\partial \phi} - \frac{\partial p}{\partial \phi} - \frac{\partial C}{\partial \phi}\right)\delta\phi = -\text{div } \varepsilon \vec{\text{grad}}\, \phi_o + q(n-p-C)$$

and solved by the same method used as if C was constant.

3 - APPLICATIONS

3.1 - GaAs semi-insulating substrate

The GaAs SI material commonly used is obtained from a residual donor doped material compensated by the chromium deep level ($E_T = E_c - .72$ eV). The Cr density can vary from $10^{16}cm^{-3}$ for low doped substrate up to $10^{17}cm^{-3}$.

Another type of SI material can be found which is called the "undoped" SI material.

The undoped material is in fact a residual acceptor doped material compensated by the E12 deep donor level defect centers ($E_T = E_c - .7$eV). For GaAs MESFET's, in both cases the active layer is obtained either by epitaxy or direct implantation. To understand the difference of behaviour of the interface space charge region between the active layer and the two different SI substrates let us

consider a $10^{17}cm^{-3}$ uniformly doped n layer and a uniform substrate in an unidimensional model. For the sake of simplicity we have neglected impurity redistribution profiles. The SI substrate is 10 µm thick.

For both substrates the residual doping densities is $5.10^{15}cm^{-3}$ (donnor or acceptor) and the deep center densities is 5.10^{16} cm-3. The ratio of capture coefficients is Cn/Cp= .1 for deep acceptors and 10 for deep donnors.

The band diagram and the density profiles at the interface for Cr doped SI at thermal equilibrium are plotted on figures 1 and 2. On the SI side of the depleted layer the charge density corresponds to the total Cr density, that is to say 5.10^{16}, since the Cr level is below the Fermi level and Cr is fully ionized.

On figures 3 and 4 same representation is done of the undoped SI case. On the SI side of the interface, due to the donor type of the deep level, E12 is not ionized so that the charge density corresponds to that of the residual acceptor density ($5.10^{15}cm^{-3}$).

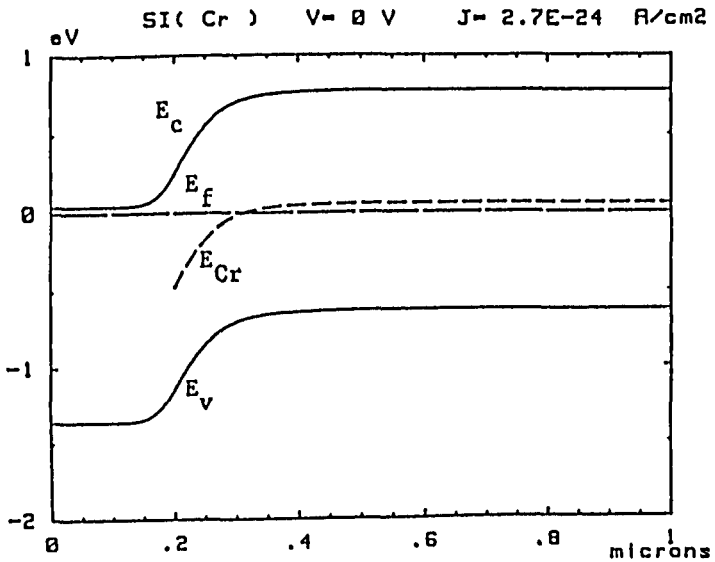

Fig. 1 : Chromium deep acceptor level in the interface junction at thermodynamic equilibrium in GaAs.

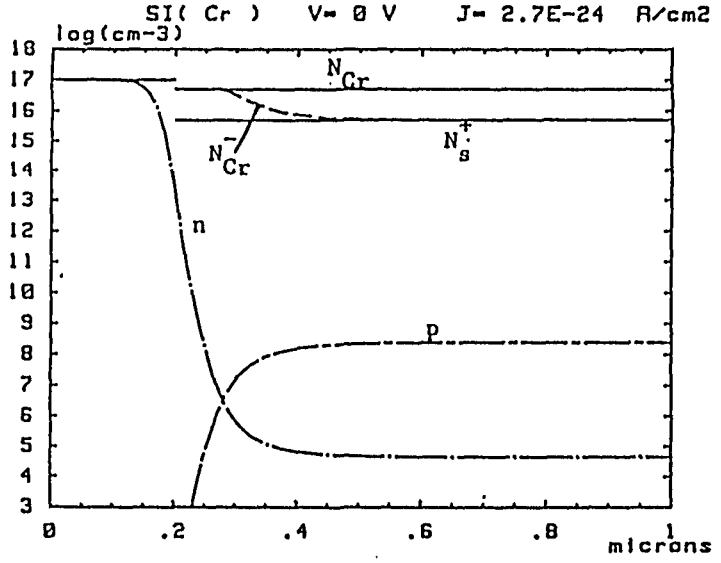

Fig. 2 : Density profiles at the interface junction for chromium compensated GaAs SI.

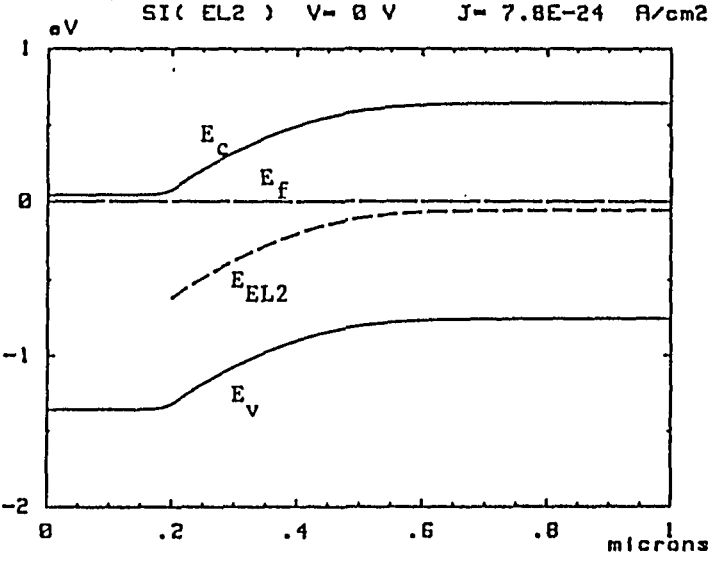

Fig. 3 : EL2 deep donor level in the interface junction at thermodynamic equilibrium in GaAs.

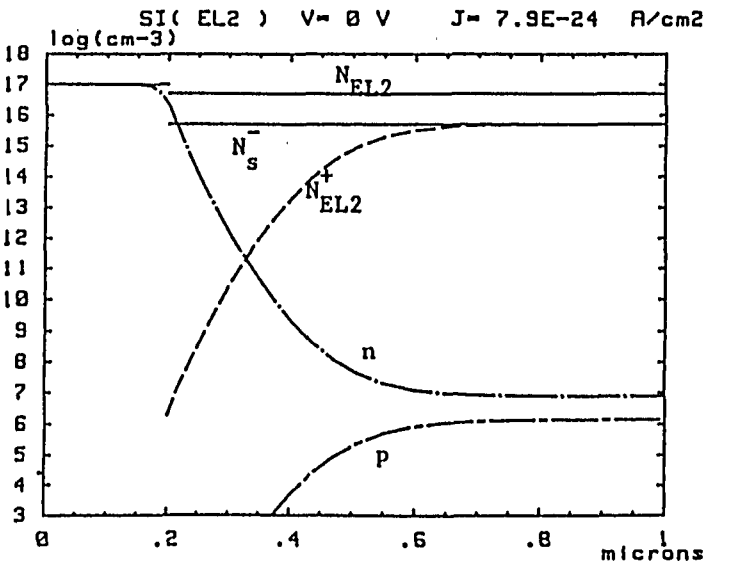

Fig. 4 : Density profiles at the interface junction for EL2 compensated GaAs SI.

It can be first concluded that the space charge region preferantially extends in the undoped SI rather than in the Cr doped SI and thus less decreases the effective active layer thickness.

On under operation FET, the source and substrate are connected to ground, whereas the drain is positively biased. Let us look at what occurs when the n type layer is positively biased.

On figure 5 the band structure of the Cr SI case is plotted for a 5 V bias. The whole voltage drop is located in the space charge region, which implies an extension of this space charge both in the SI material and in the active layer. The active layer thickness thus decreases.

In the undoped SI case, described on figure 6, for the same bias conditions, the voltage drop spreads through the whole of the SI material which behaves as a resistance. No extension of the space charge region is found. But, if in the case of the Cr doped SI the computed leakage current was 2.10^{-9} A/cm^2, the leakage current is now 10^4 time greater for the undoped SI case. Whether this current is negligeable or not depend on the structure of the device and its application.

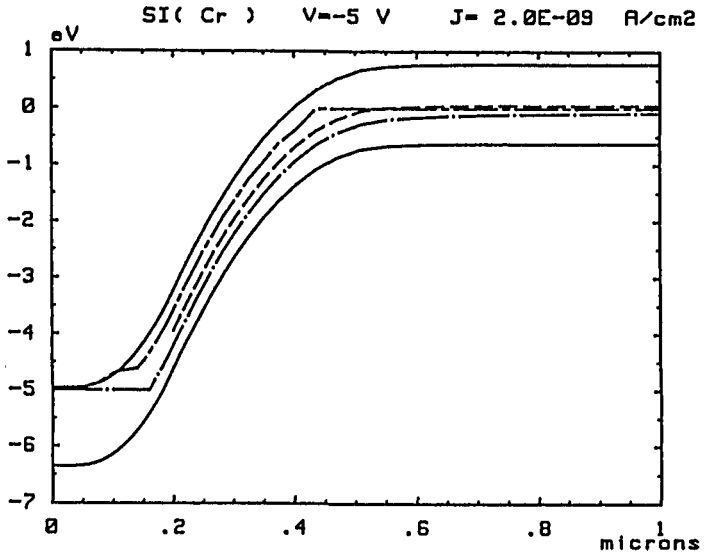

Fig. 5 : Behavior of the n-SI structure under 5V reverse bias for Cr in GaAs.

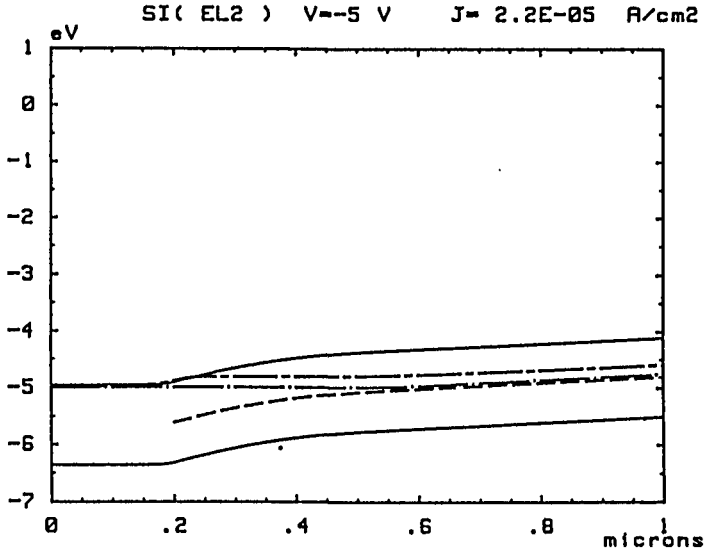

Fig.6 : Behavior of the n-SI structure under 5V reverse bias for EL2 in GaAs.

3.2 - InP semi-insulating substrate

The InP semi insulating material commonly used is obtained from a residual donor doped material compensated by Iron (Fe) deep acceptor level (E_c=E - 0.56eV). In that case the active layer consist of an epitaxial GaInAs layer leading to a heterojunction.

The description of the band structure at thermal equilibrium and under a 2 V bias is given on figures 7 and 8. The thickness of the SI substrate is 10 µm. It can be seen on fig. 8 that this type of structure behaves in an intermediate way to the Cr doped an EL2 GaAs SI. That is to say half of the bias increases the space charge region while the other half is spread over the 10 µm of substrate.

The respective extension into the active layer and into the SI material depends on the ratio of the active layer doping and iron density.

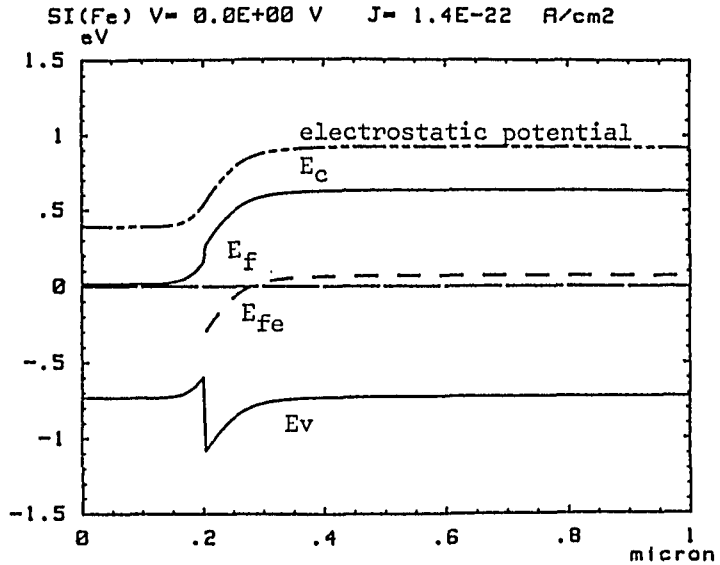

Fig. 7 : Fe deep acceptor in the interface heterojunction at thermodynamic equilibrium in InP.

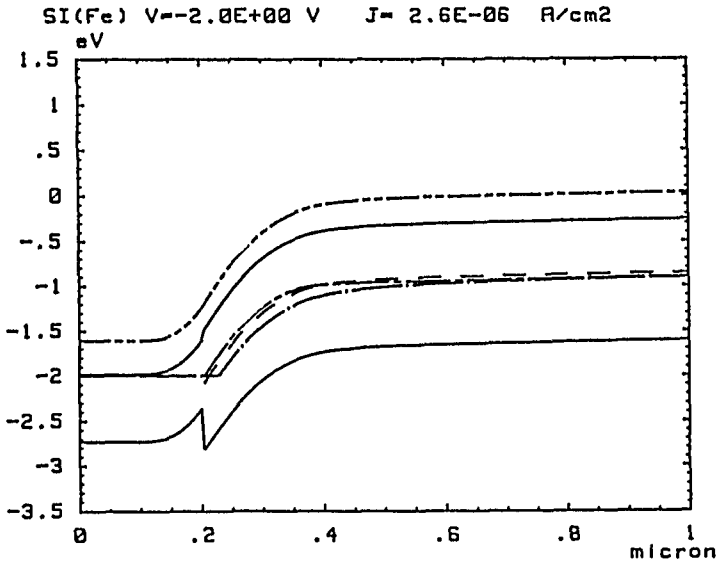

Fig.8 : Behavior of the GaInAs InP SI structure under 2V reverse bias.

3.3 - FET bidimensionnal simulation including semi-insulating substrate

As an example we simulate a scholar JFET which consists of a 10^{17} cm^{-3} GaInAs n layer on a Fe InP SI substrate. The junction under the gate is obtained by a 10^{17} cm^{-3} p layer. Geometry of the device is given figure 9.

The three dimmensional representation of the electrostatic potential surface, at thermal equilibrium is given on figure 10. The corresponding electron density surface is described Figl1.

It must be pointed out that these surfaces distort the real geometric dimensions of the device. The non uniform mesh is here described by representing each cell of the mesh by an equal projected surface.

The location of space charge regions can be seen on these figures.

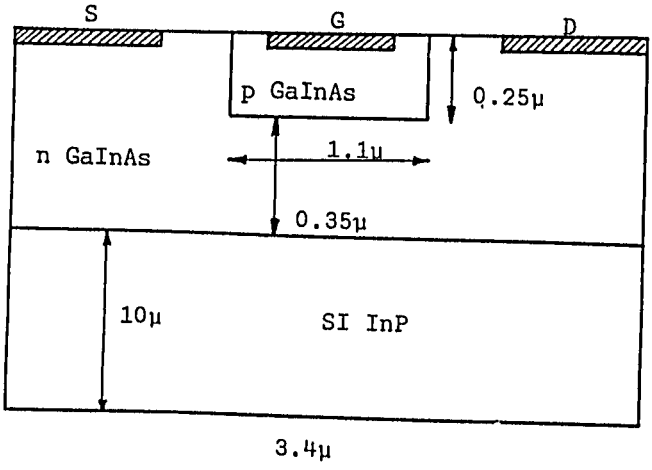

Fig. 9 : Structure of the simulated JFET.

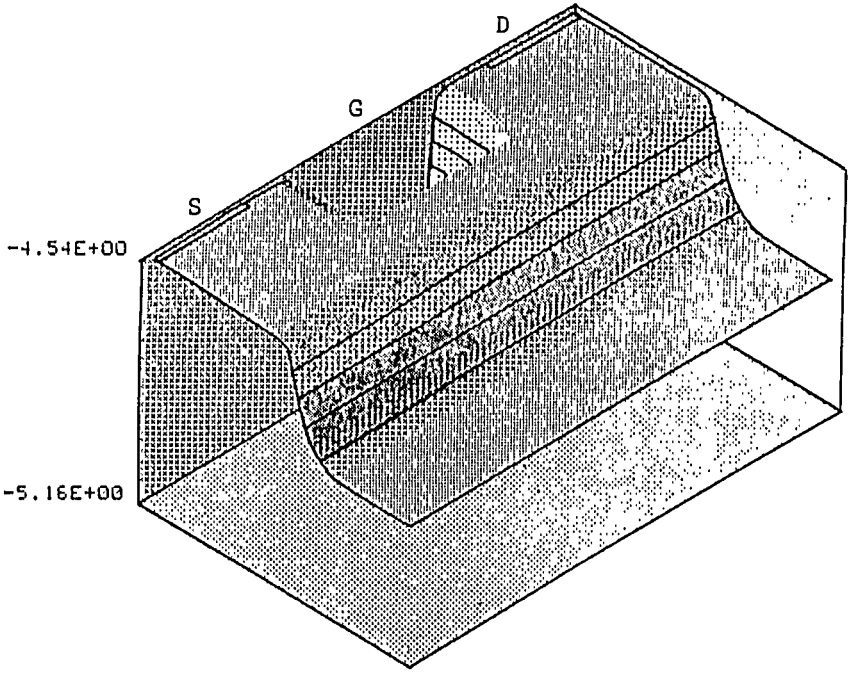

Fig. 10 : Electrostatic potential map at thermodynamic equilibrium.

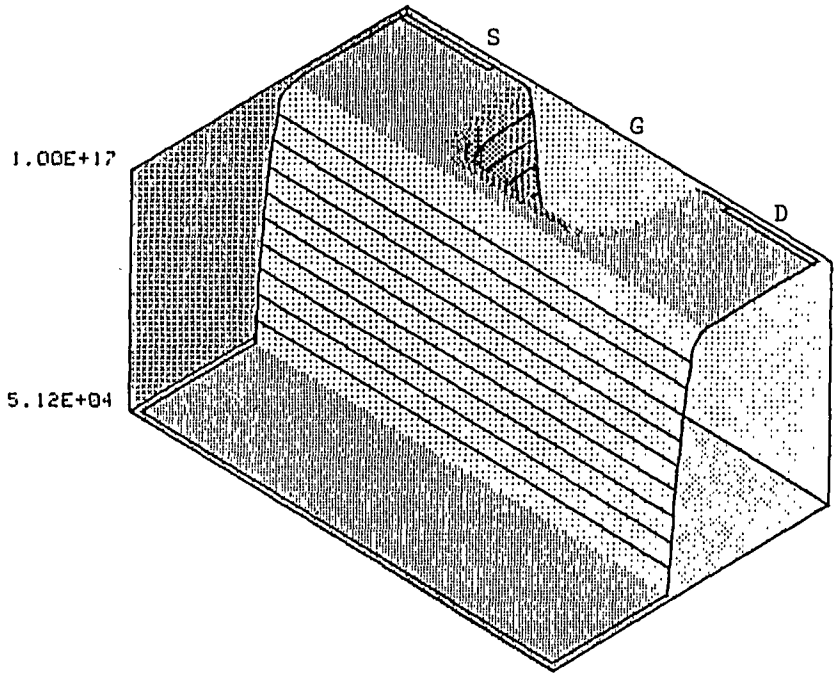

Fig. 11 : Electron density map at the thermodynamic equilibrium

The JFET is now biased under saturation conditions with Vds=1.5 V.

The electrostatic potential, plotted figure 12, shows the extension of the space charge region, below the drain, into the SI substrate.

So as to unterstand the behaviour of the component, the amplitude of the norm of the electric field surface has been drawned on figure 13. It shows the major high field areas corresponding to the space charge region and their respective importance. We can then understand that the channel thickness is controlled both by the gate space charge region and by the interface space charge region. The small "high electric field " region at the drain side of the channel describes saturation.

The next figure 14 shows the electron density surface on which we can see the accumulation depletion of electron density at the exit of the channel; as well as the extension of the space charge region under the drain which leads to a decrease of the effective active layer width.

On figure 15 is plotted the doping density which corresponds to the total ionized impurity density. It can be remarked, the totaly ionized region of the SI under the drain corresponding to the extend of the space charge region.

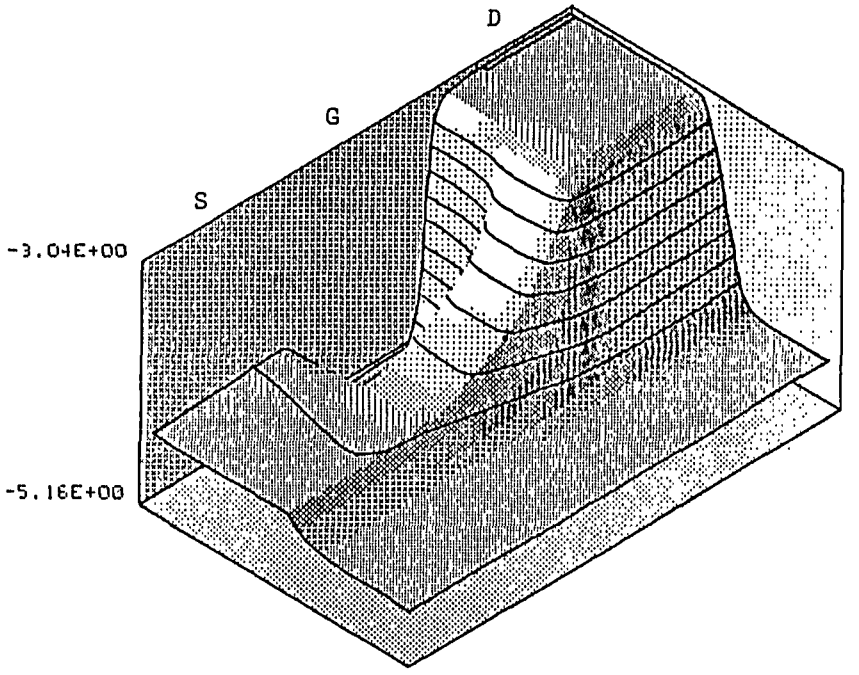

Fig. 12 : Electrostatic potential map for V_{DS} = 1.5V

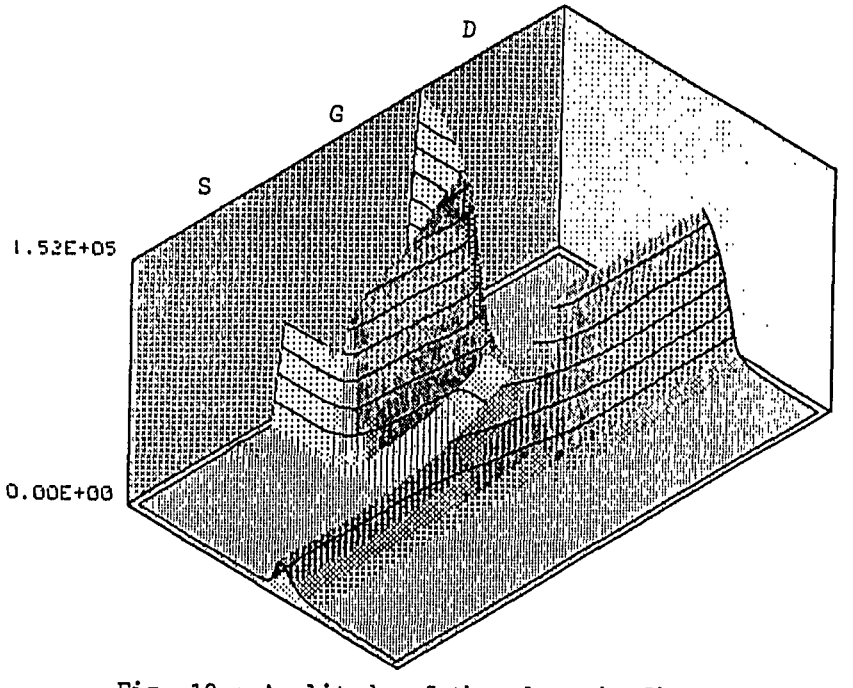

Fig. 13 : Amplitude of the electric field map for V_{DS} = 1.5V.

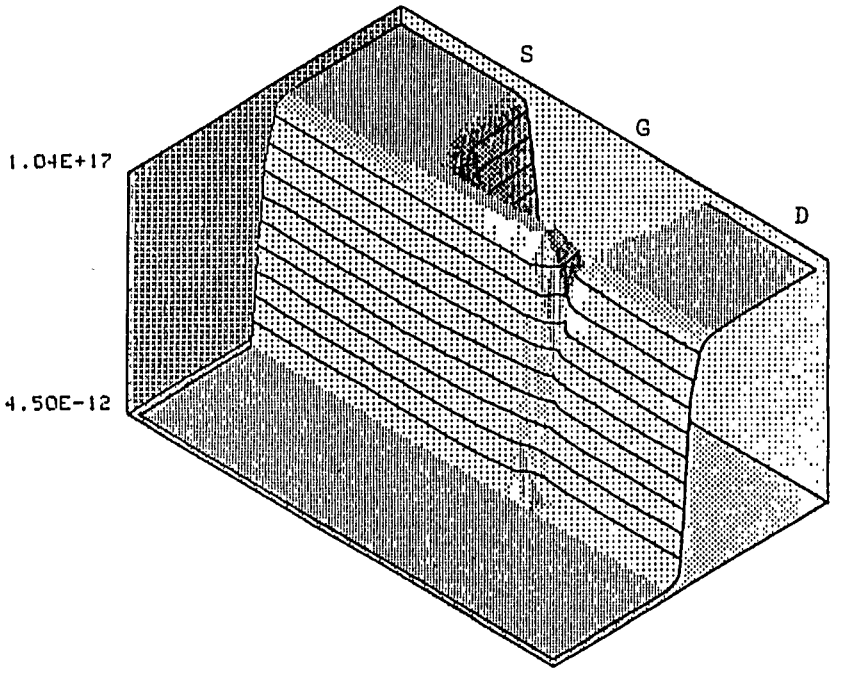

Fig. 14 : Electron density map for V_{DS} = 1.5V.

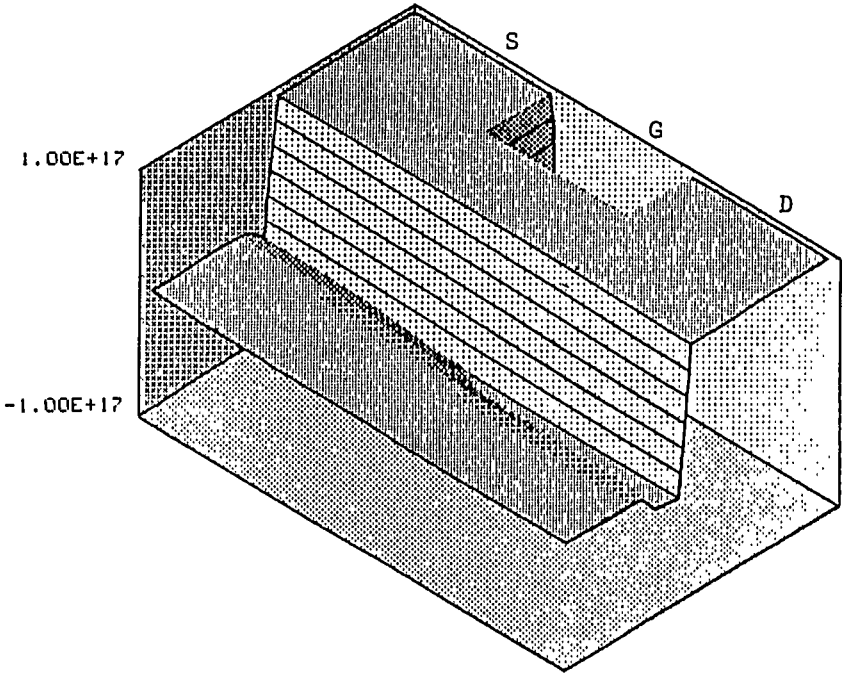

Fig. 15 : Net ionized impurity density for V_{DS} = 1.5V.

4 - CONCLUSION

We have shown that III.V FET simulation must take into account the semi-insulating substrate behaviour.

The semi insulating material equilibrium model is simple enough to be included in the general transport set of equation using the electrochemical and electrostatic potentials representation

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