THE NUMERICAL SIMULATION OF SILICON-ON-INSULATOR MOS DEVICES

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Abstract

In this paper the differences between MOSFETs fabricated in a silicon-on-insulator (SOI) and in a bulk silicon technology are discussed along with examples of applications of simulation techniques to SOI devices. These examples include the calculation of the magnitude of the parasitic capacitances which become important in low capacitance SOI technology, calculation of the influence of the edges of a device on its behaviour, calculation of the threshold voltage of an SOI device and calculation of the 'substrate' potential in an SOI device using two dimensional simulation. For most of the examples, silicon-on-sapphire (SOS) technology has been chosen to illustrate the methods used.

Although broadly the same simulation techniques can be applied to both bulk and SOI technnologies there are subtle differences of application which are discussed. This is most clearly visible when calculating the current flowing in an SOI MOSFET using two dimensional simulation where the numerical problems associated with a floating substrate region cause the problem to be very ill-conditioned.

The difference between the physical parameters required for the simulation of SOI rather than bulk devices is discussed. This includes the nature of the silicon film which will affect both carrier mobility and carrier lifetimes, and that of the front and rear interfaces of the silicon which can affect the device operation.

Introduction

Silicon-on-insulator technology is arguably the silicon technology of the future. If it does replace conventional bulk

silicon MOS technology it will be because it provides the ability to build large systems on one chip by stacking subsytems vertically on the same substrate. This is achieved by fabricating a base level of devices on a substrate and then covering them with an insulating layer, depositing a new layer of silicon over the insulator and building the next layer of devices in it; etc. Silicon-on-insulator technology is, however, not new; it's history can be traced back to the late 1960's when silicon MOS devices were manufactured in thin layers of silicon deposited on a crystalline insulator (sapphire or spinel [1]). With these devices it was hoped to improve the electrical insulation between neighbouring transistors as well as to reduce the parasitic capacitances (present in all bulk silicon technology between wiring or source/drain diffusion and the substrate) to obtain a consequential speed improvement and power reduction. The high cost of the substrates used in this approach has limited the use of such technology to high performance military and space applications.

With the growing interest in silicon-on-insulator (SOI) technology it seems timely to consider the simulation of MOS devices in SOI as they do indeed pose interesting problems to both the device physicist and numerical analyst. I will, in the main use silicon-on-sapphire (SOS) MOS devices as an example of SOI technology as it is the most mature with approaching a dozen companies currently manufacturing SOS devices. I am confident similar consideration is required for all SOI technology.

The SOI Device Structure

There is as yet no universally accepted choice of insulator or method of growing the silicon on it; these are very much current technological problems. Isolation between devices is obtained either by etching the silicon away to leave each device in its own silicon island (mesa structure) or by local oxidation to give a planar structure. In the former case the devices will have edge properties not seen in bulk MOS devices. The transistors are fabricated in this silicon layer using conventional MOS techniques of oxide growth, gate deposition, ion implantation etc.

Figure 1 compares the basic n-channel MOS device structure for SOI and bulk substrates. Although there are many similarities between the structures the following differences affect the operation of the devices:

The SOI device is usually made in a layer of silicon sufficiently thin that both the source and drain (including their depletion regions) reach the back of the film. This eliminates parasitic capacitance at the junction bottom.

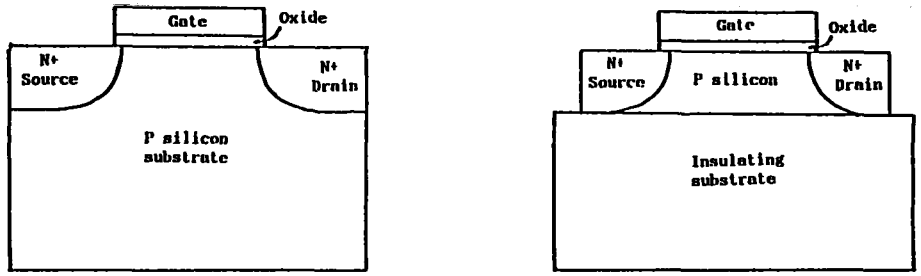


Figure 1 Comparison of silicon-on-insulator and bulk silicon MOS device structures

At the back of the silicon film there is a silicon-insulator interface which is usually sufficiently close to the surface to affect the device operation.

The P silicon beneath the channel does not naturally have a contact to define its potential. For bulk devices a contact to the back of the wafer defines the substrate potential.

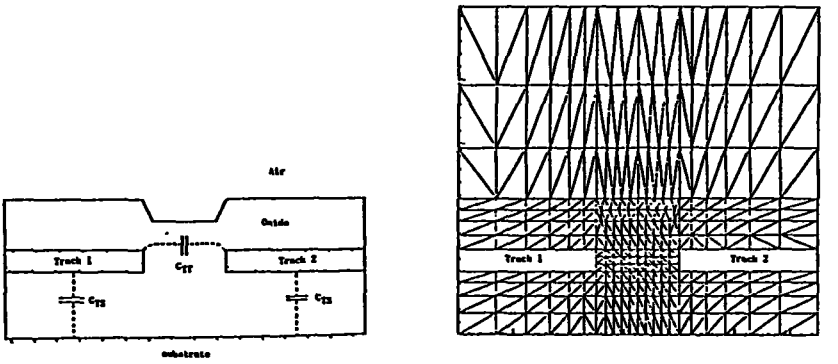
For a mesa device the island edge will define the device width (into the paper in fig 1). For narrow devices conduction processes along the edge between source and drain can influence the device characteristics.

The growth of a thin layer of silicon on insulator is technologically more difficult than the growth of single crystal silicon. Thus it is normal to pay a penalty in SOI technology which takes the form of a stressed film with a higher defect level. These factors affect the carrier mobility in the film and also the recombination lifetimes. For SOS technology, the surface electron mobility is usually some 30 % lower than that in bulk, whilst the hole mobility is little changed (stress actually enhances hole mobility [1] and compensates for the reduction caused by defects); carrier lifetimes fall off towards the back of the film where the defect density is highest, values of the order .1 ns are not untypical [2]. The low lifetime explains why bipolar devices are not made in SOS technology.

The Simulation of Wiring Capacitances in SOI Technology

SOI technology offers a speed advantage over bulk technology when the lower capacitances due to the removal of source/drain junction bottom capacitances and the reduced wiring capacitances offset any reduction in the carrier mobility in the device. To maintain the speed advantage it is important to know the factors controlling the parasitic capacitances. For SOS technology where the insulator also forms the physical

substrate and hence is several hundred microns thick, the capacitance between neighbouring conductors will be controlled by the thickness and the separation of the conductors whilst the capacitance to the contact at the back of the insulator is negligible. For an SOI technology where the insulator thickness can be varied (e.g. regrown silicon on oxide-upon-silicon) the parasitic capacitance value and the way it is distributed between inter-track (C_{TT}) and track-to-substrate (C_{TS}) capacitance (Fig 2a) become process dependent.



a/physical structure b/simulation mesh

Fig 2 Inter-track parasitic capacitances in SOI

The value of these capacitances can be obtained by the solution of Laplace's equation in two dimensions using a finite element device simulator. (Arguably a boundary element technique is better for this purpose, but the exploitation of the device simulator is more convenient.) Fig 2b shows an example of a triangular mesh used to solve for the inter-track and track-to-substrate capacitances. Experimentation with the mesh ensures that the mesh is adequately fine and the boundaries are sufficiently far from the contacts (tracks) to yield accurate results for the capacitance. The potential distribution is then obtained by discretising the Laplace equation using a Galerkin method and solving the resulting linear equation using ICCG(0). The charge on each contact can be calculated by integrating the electric displacement normal to the contact thus:

$$Q_i = \Gamma_i \int \epsilon\epsilon_o \ \underline{E}.d\underline{\Gamma}$$

The capacitances can then be calculated by independently varying all but one contact's potential and noting the change in nodal charge. Thus the capacitance between nodes i and j (C_{ij}) is given by:

$$C_{ij} = dQ_i/dV_j$$

The effect of varying the insulator thickness for a silicon-on-oxide technology is illustrated in the simulation results shown in fig 3 where the total capacitance at the output node of an inverter cell due to track-to-track and track-to-substrate capacitances is shown as a function of oxide thickness. The inverter was designed to 1.5μm rules for a technology with 25nm gate oxide. For comparison the gate capacitance of the inverter and the corresponding capacitance for a SOS technology are shown. The graph shows that for a thin insulating oxide the parallel plate capacitance to substrate dominates but as the oxide thickness becomes comparable to the separation of the interconnect (1.5μm) then lines of force can deflect from the substrate towards the neighbouring track and the capacitance to substrate and the capacitance between tracks becomes comparable. For even thicker oxides the parallel plate capacitance reduces to zero and the parasitic capacitance becomes dominated by the track-to-track capacitance as happens in SOS technology. Thus choosing an insulator of thickness close to the design rule dimension will give rise to a low parasitic capacitance without increasing the crosstalk capacitance due to the track-to-track component unnecessarily. It can be seen that in silicon-on-oxide technology the parasitic capacitance can be reduced to about one half of the gate capacitance; this is better than can be achieved with a bulk technology (due to junction bottom capacitance) or even a SOS technology (due to the high dielectric constant of sapphire).

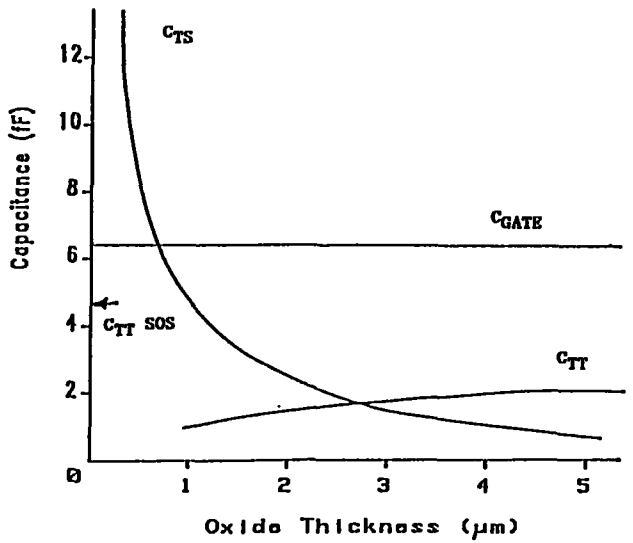


Figure 3 Simulated capacitance variation with underlying insulator (oxide) thickness

The Simulation of the Effect of Edges on Device Performance

The width of SOS transistors manufactured using a mesa technology is defined by the island edge. To simulate the effect of the edge on conduction between source and drain a three dimensional simulator is required. However much useful information can be achieved from a solution of Poisson's equation across the device's width with the carrier Fermi levels set to zero throughout the island. This is equivalent to setting the source and drain bias to zero and then exploiting the translational symmetry along the device. Clearly this simulation cannot directly give information about the current, however, an investigation of the distribution of minority carriers within the silicon as a function of gate bias will indicate where current will flow if a small drain bias is applied. Figure 4 illustrates the idealised edge structure that I will use to illustrate the edge properties of a SOS transistor.

Poisson's equation is solved on the finite element mesh shown (only one half of the device need be solved as it is symmetric about the centre plane). The Laplace operator is discretised using linear shape functions whilst the charge due to background doping and carriers is evaluated at each node and included in the discrete equations by a box-integration procedure around each node. The carrier density depends exponentially on the potential through the Boltzmann statistics thus making the equation set extremely non-linear. A Newton technique damped by the method of Bank & Rose [3] provides an efficient solution method. The discretisation used ensures the linear equation set solved at each Newton iteration has a symmetric, stable, diagonally dominant, positive definite matrix which can efficiently be solved using ICCG(0).

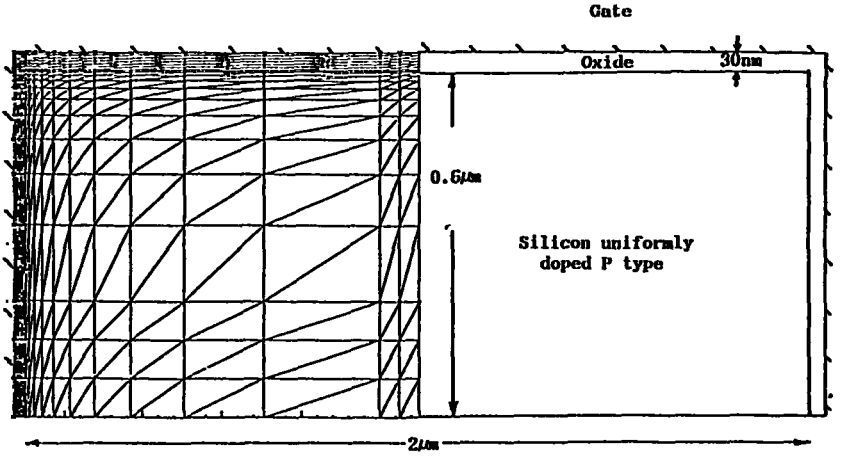
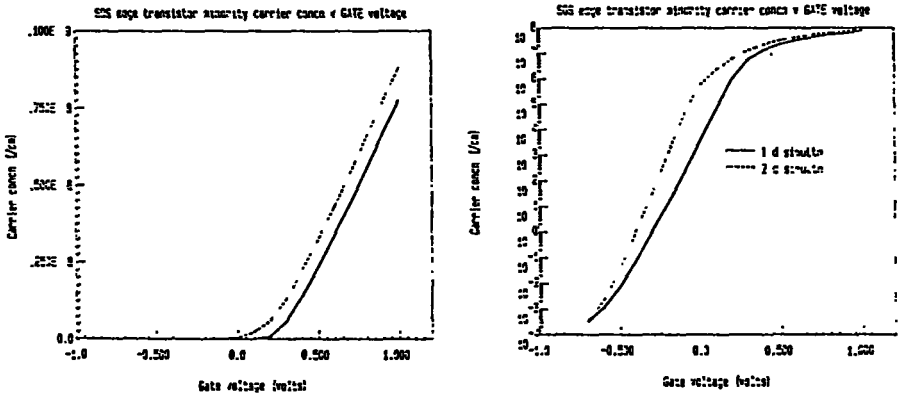


Fig 4 Structure and mesh for simulation of transistor edge

To analyse the results of the simulations, the total electron density in the silicon island is obtained by integration over the device for a range of gate voltages. The integrated electron density can then be plotted against the gate voltage (Fig 5a) to simulate the onset of strong inversion in the linear region of device operation or a log-linear plot can be drawn (Fig 5b) to simulate the subthreshold conduction. In both these figures the minority carrier density in an edgeless device (of width equal to the sum of the width and twice the height of the edged device) is presented for comparison.



a/ linear region b/ logarithmic (subthreshold)

Figure 5 Simulated minority carrier dependence on gate voltage

Fig 5a shows that the presence of the edge has given rise to an effective lowering of the threshold voltage by about 100mV. This is due to a sharing of the charge in the depletion region at the corner by both the gate at the top of the device and that at the side; this then allows the gate to support an increased electron density at the corner. Since the extra charge is only at the corner, its effect on the threshold voltage will decrease as the device gets wider. The results of measurements of the width dependence of threshold voltage on N-channel SOS are shown in figure 6. Although these devices cannot be expected to possess either the ideal structure or doping used in the simulation they show both the expected trend with width and a comparable value of shift.

Fig 5b shows that the edged device not only shows a

lowered threshold but also the carrier density falls off less rapidly just below threshold than for the edgeless case. This can be identified as due to the retention of carriers at the corner due to the joint effect of attraction to the top and edge gate. In practice such a mechanism will be obscured by the true edge and corner profiles. Moreover variation in the doping and interface charge along the edge determine the its contribution to the subthreshold slope. However this example shows how simple simulation can be used to investigate the contributions of the edge to conduction in an SOS device.

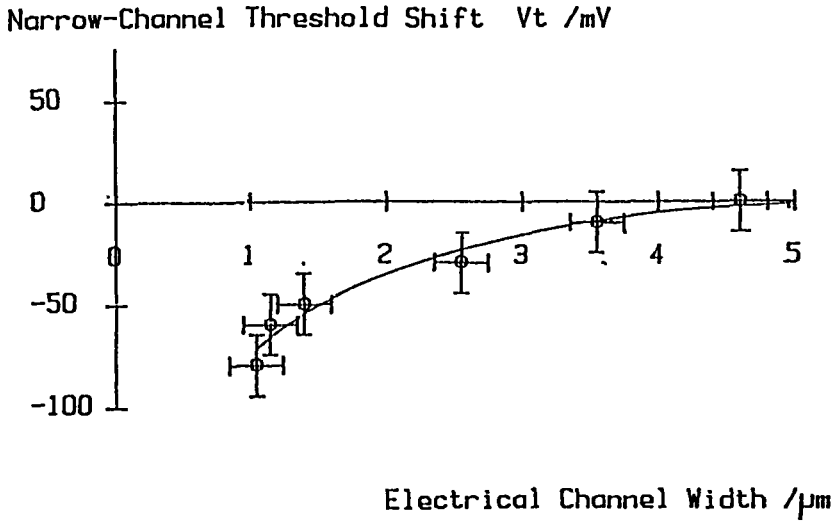


Figure 6 Measured width variation of threshold voltage for n-channel SOS devices

The Threshold Voltage of SOS Transistors and the Effects of Interface Charge

The SOS transistor can operate in one of two modes. Firstly, the surface depletion region may not extend right to the back of the film. In this case there will be a space charge neutral region behind the surface depletion region. The potential of this region will be determined by small currents flowing between source and drain through this region. The potential therefore floats and the region is known as the 'floating substrate'. Behind the floating substrate a second depletion region can also exist, this will be induced by charge at the silicon-sapphire interface. Thus the presence of the floating substrate will be determined by the thickness of the silicon film, the doping and the rear interface charge density. Alternatively the device operates in a fully depleted mode when the rear interface charge will directly affect the threshold voltage as there is no floating substrate to screen the charge.

Ideally, the back interface properties should be well

understood before simulation of the threshold can be made. For SOI technologies where the insulator is reasonably thin ($\lesssim 5\mu m$) it is possible to investigate the back interface by looking at the properties of the transistor formed at the back of the silicon with the insulator acting as the controlling dielectric. If the insulator is too thick then the voltages that must be applied to control the transistor become restrictively high and the capacitance that must be measured during C-V experiments becomes too small. To date only limited experimental work has been carried out on SOS technology [4] by thinning the substrate and using kilovolt power supplies.

Since we don't have a good knowledge of the rear interface charge for SOS films we must use simulation combined with threshold voltage measurement to tell us something about the interface charge. This is most conveniently achieved by investigating the substrate bias dependence of threshold voltage using a special device structure that enables contact to be made to the floating substrate whenever it exists. If the device has a floating substrate, then as the substrate bias is applied, the surface depletion width increases and the threshold voltage increases until the front and rear depletion regions meet; it then remains constant. At this point a fully depleted mode of operation exists and the rear interface charge directly affects the threshold voltage and hence can be calculated. This is illustrated in fig 7 which compares the substrate bias dependence of the measured threshold voltage of an N-channel SOS transistor (35nm gate oxide, $0.6\mu m$ silicon film, with the silicon doping controlled by twin implants at the front and back of the film) with that simulated for two different fixed interface charges. The latter results have been obtained by

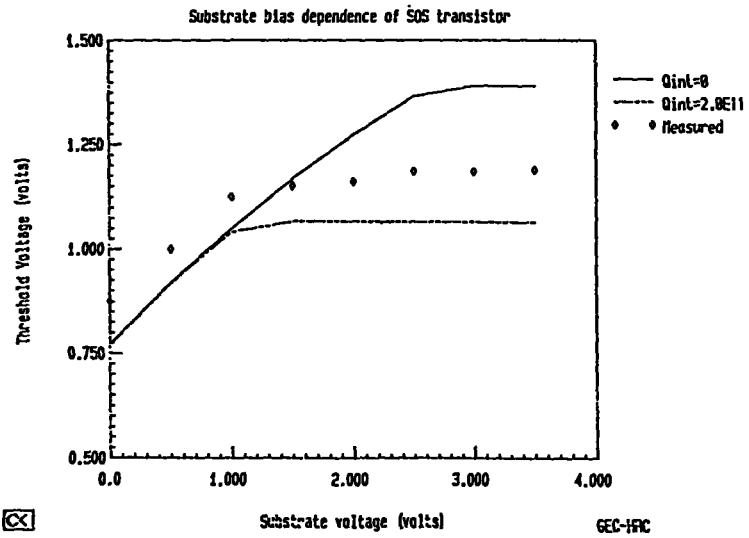


Figure 7 Measured and simulated substrate bias dependence of threshold voltage

a solution of Poisson's equation in one dimension, calculating the threshold voltage by investigation of the gate bias dependence of minority carrier density, and simulating back bias by varying the hole quasi Fermi level throughout the silicon whilst keeping the electron quasi Fermi level fixed. The simulation shows a good agreement with measurement if a fixed charge of around $2.10^{11}cm^{-2}$ is assumed; the offset in threshold voltages without substrate bias (≈ 0.1 V) is attributed to small uncertainties in the knowledge of the doping profile.

Again this procedure illustrates how a low dimension simulation can be applied to investigate threshold voltage variations in an SOI device. However it does not allow a distinction to be drawn between fixed interface charge, interface traps and pinning of the potential at the interface.

Two Dimensional on-state Simulation of SOI Devics

a/ Numerical Problems

The simulation of SOI devices can be achieved by solving for the distribution of potential and carriers within the device that is consistent with Poisson's equation and the current continuity equations for the bias applied. This is, in principal, the same approach that is used for silicon MOSFETs (e.g. ref[5]). For SOI devices with floating substrates the solution of these equations is more difficult than for bulk devices because of the poor condition of the equations. In this section, I wish to explore the reasons for the difficulty in solving the equations using an engineering approach to the operation of the device.

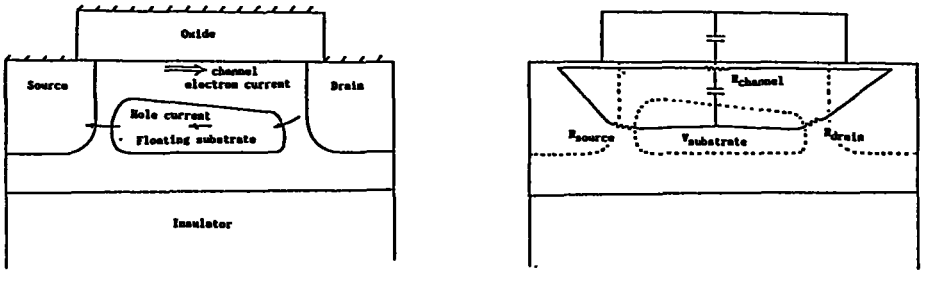


Figure 8 Paths of current flow in an SOI device with a floating substrate

Fig 8 illustrates the passage of current within an n-channel SOI device. The total device current contains two contributions, firstly the channel current due to the motion of

electrons which is typically of the order 1A per cm of device width. Secondly, the hole current flowing through the substrate due to generation in the drain region and recombination in the source region. The magnitude of this current will be determined by the carrier recombination lifetimes for low drain biases but will be dominated by avalanche generation at higher biases. For SOS devices where the carrier lifetime is of the order 1ns, the substrate current is of the order 10^{-8}A per cm of width at low drain biases.

At first sight it seems that the second current can be neglected in the solution; however, it is this small current that determines the potential of the floating substrate region which adjusts until the drain generation current exactly matches the source recombination current. Through the depletion capacitance between the floating substrate and the channel, the floating substrate potential directly controls the flow of current in the channel (this is essentially back gate bias). Thus to get an accurate measure of the channel current it is important that the substrate potential has converged adequately and hence the substrate current must be well solved. Furthermore, in the floating substrate region, the Poisson equation can be upset by relatively small changes in the quasi-Fermi levels, whilst in the fully depleted case, it is dominated by the fixed charge; this strengthens the coupling between the Poisson and current continuity equations. This coupling and the need to be able to have confidence that the potentials have converged adequately throughout the device suggest that a simultaneous solution strategy using a Newton-like algorithm with known convergence properties is used. Other authors (e.g.[6]) have used a modified sequential (or Gummel) strategy to solve the equations successfully. Although I will now focus on the simultaneous approach, the arguments can be applied to others.

There are two numerical problems associated with this solution. Firstly one of numerical resolution in the substrate. To resolve a current (J) of the order 10^{-8} Acm^{-1} in a substrate of thickness (t) $\approx$ 1μm with a carrier mobility (μ) of $1000cm^2V^{-1}s^{-1}$, and doping density (N) of 10^{16} cm^{-3}, the mesh must be able to resolve a potential gradient of:

$$E = J/(q.N.\mu.t) = 6.25\ 10^{-5}\ Vcm^{-1}$$

In the presence of built-in potentials of about 1V. with typical mesh spacings of about 0.1μm this requires a numerical precision of about 1 in 10^9; thereby ruling out REAL*4 calculation and indicating that devices with lower substrate current, because of improved lifetimes, may even approach the resolution of REAL*8 floating point numbers.

Secondly, this particular problem is very ill-conditioned because the linear problem obtained in the Newton scheme has

In practice, to get a solution of the floating substrate problem, it is necessary to ensure that the initial guess prior to the start of a Newton solution procedure does not introduce too large an error in the substrate potential; to achieve this we ensure that the substrate is held at source potential during the initial guess. It is then important that the linear equations are well solved at each iteration; whilst retaining an iterative scheme we ensure that the residuals of the equation have been reduced by a factor of 10^8, in a suitable norm, at each iteration. This has been found to restore quadratic convergence starting at updates of magnitude 1 thermal volt in all practical problems to date. This allows reliable solution of floating substrate problems but is more expensive than the solution procedure for normal MOS devices.

b/ Simulation of the Floating Substrate Potential in Two Dimensions

Fig 10 shows the doping profiles and device structure for an SOS device. The device has a 35nm gate oxide, a 0.6μm thick silicon film and is 3μm long. To represent the reduction in quality of the film, peak surface mobility values of 300 $cm^2V^{-1}s^{-1}$ for electrons and 200 $cm^2V^{-1}s^{-1}$ for holes have been used, the value for electrons is some 40% lower than that in a bulk device. A uniform value of 0.1ns for both carrier lifetimes has been assumed, which whilst representative of the worst case lifetimes reported in [2] does not attempt to represent the variation of lifetime through the film. To complete the definition of the problem, dielectric constants of 11.7 for silicon, 4.0 for oxide and 10.0 for sapphire were assumed. This high value for sapphire accounts for the strength of coupling via parasitic capacitances in SOS technology.

A bias of 3V was applied to the gate, this will ensure the device is operating about 2V above threshold whilst a drain bias of 1V is applied. This biases the device into the linear region of operation, thus high fields will not be present at the drain and the drain-substrate current will be dominated by thermal generation. To look at the effect of this current on the substrate potential, fig 10 shows a plot of the hole Fermi-level along the line EF which is chosen to intersect the substrate. (It is preferable to inspect the majority Fermi-level rather than the electrostatic potential as interpretation of the latter is confused by a doping dependent built in voltage.) This plot indicates that the potential has risen some 0.2V above the source potential to ensure that the substrate-source diode is sufficiently forward biased to sink all the drain generated current. This clearly illustrates the floating substrate mechanism.

a very small eigenvalue. This can be seen since, for the current continuity equations, the matrix of the linear problem relates a change in potential in the device to a change in current. For an n-channel device the floating substrate can move up and down by quite a large potential without making a significant difference to the hole current continuity equation because of the high resistance of the diodes between substrate, source and drain. The solution of the linear equation set therefore becomes much more difficult and an iterative technique based on conjugate gradients will initially reduce the residual of the linear equation set without correctly adjusting the floating substrate potential.

This manifests itself in a Newton iteration scheme that appears to converge nicely down to about .01 thermal volts and then, as the residual of the nonlinear equation becomes dominated by the desire to change the substrate potential, much larger updates are required. The non-linearity of the problem, however, is such that these large updates cannot be accommodated by the damping scheme and slow convergence is obtained. This is mathematically explained in ref[7] where it is shown that the onset of quadratic convergence can start much closer to the final solution for a poorly conditioned problem than a well conditioned one. This is undesirable as without some guarantee of the convergence behaviour it is not possible to state with confidence how accurately the floating substrate potential is known.

This behaviour can be visualised (fig 9) by conceptually converting the solution of the set of non-linear equations to a problem of minimising their global magnitude. In this case, we can track the solution down into a valley with a shallow bottom (corresponding to the low eigenvalue). Unfortunately the valley bottom does not follow a straight path to the global minimum (zero) but bends due to the non-linearities.

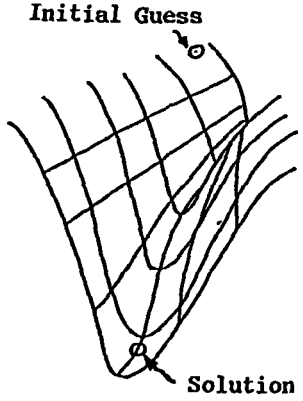
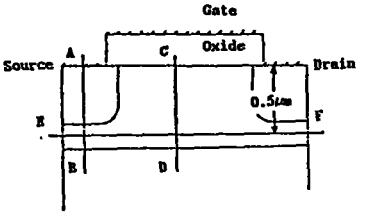
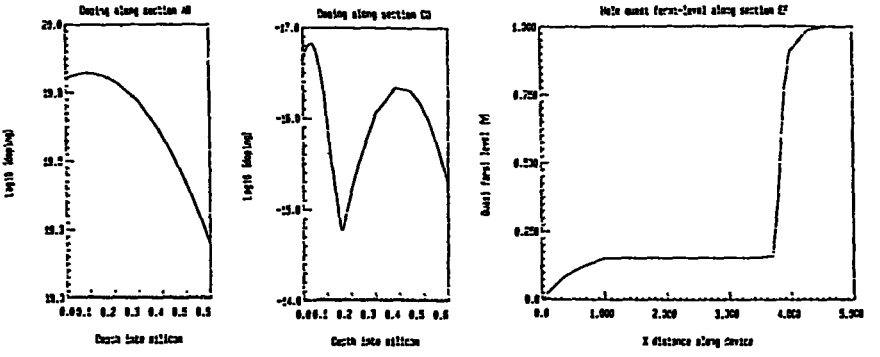


Figure 9. A schematic illustration of the path towards solution in an ill conditioned non-linear problem

a/ Device structure





b/ source/drain doping profile

c/ channel doping profile

d/ Potential through the floating substrate

Figure 10 Simulation of the floating substrate potential in an n-channel SOS device

Conclusions

In this paper I have outlined the structure of an SOI MOSFET and illustrated its operation. Numerical simulation can be applied to many aspects of the SOI device to help in the understanding of the device performance. These have been illustrated with examples of parasitic capacitance simulation, edge transistor operation, threshold voltage calculation and finally the calculation of current flowing in the device using two dimensional simulation. The techniques although broadly similar to the techniques applied to conventional MOS devices are subtly different in their application; this is most pronounced in the calculation of current flowing in an SOI transistor with a floating substrate, where a severe ill-conditioning of the equation to be solved requires extra care and computation time.

Finally, it has been noted that the nature of the thin silicon film and the interfaces introduce differences in the

physical parameters which control the operation of the device. In particular the mobility of carriers in the film will be controlled by technological factors as will carrier lifetime and the charge present at the interfaces of the silicon. All these factors can control the operation of the device and therefore need 'calibrating' for the technology under investigation.

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