R_{ON} - BV - C_{GD} COMPROMISE IN POWER VDMOS TRANSISTORS

M. LE HELLEY, J.P. CHANTE

Laboratoire d'Electronique, Automatique & Mesures Electriques
U.A. (C.N.R.S.) n° 848 - Génie Electronique
ECOLE CENTRALE DE LYON
36, av. de Collongue - BP 163 - 69131 ECULLY Cedex - France

Summary

The compromise between the on-state resistance, the breakdown voltage and gate-drain capacitance of power V_{DMOS} transistors is studied by numerical methods. Devices with a N-diffused zone and an oxide step on the top of the epi-layer are presented. The total area of the device can be decreased while R_{on} is kept constant. An improvement of R_{on} equal to 50 % is obtained ; an optimum value of the oxide step height to reach a maximum breakdown voltage for a given on-state resistance is determined.

Notations

R_{ON}	On-state resistance neglecting channel resistance
BV	Breakdown voltage
C_{GD}	Gate-drain capacitance per cm^2
BV_{voi}	Breakdown voltage of ideal plane junction
N_{SP+}	Surface impurity concentration of P^+ diffusion
N_{SP}	Surface impurity concentration of P diffusion
N_{epi}	Impurity concentration of N-epi layer
V_{DS}	Drain-source bias
ρ	Resistivity
q	Electron charge
μ_n	Electron mobility
C_{ox}	On-state gate-drain capacitance
ϵ_{ox}	Absolute permittivity of oxide
V_G	Gate bias
V_i	Potential at node i

1. Introduction

A major problem when designing power VDMOS is the determination of the best R_{ON}-BV compromise by the proper choice of the structure parameters. An other feature of power VDMOS transistor is the capacitance C_{GD} between the gate and the drain and minimizing this capacitance is of first importance. This paper is concerned with the R_{ON}-BV-C_{GD} compromise in VDMOS transistors. A structure is presented for which R_{on} and C_{GD} are decreased while holding BV at a proper level. Numerical simulations are used to determine the optimum values of the device parameters.

2. Simulated structure

The structure we have studied is a n-channel VDMOS, it is shown in Fig.1. The N zone between the P-regions is intended to decrease the pinched component R_{JFET} of R_{ON} [1]. To decrease the capacitance C_{GD} a step in the oxide is formed in front of the N-epitaxial zone but the gate overlap is conserved. Indeed, this gate overlap acts as a protecting field-plate for the curved part of the p-n junction formed by the channel region and the N-epi layer, thus increasing the breakdown voltage. High voltage devices (BV_{VDI} = 500, 1000 and 1500 volts) have been studied, but only the results on the 500 volts structure are presented here. Similar results are obtained for the other two structures.

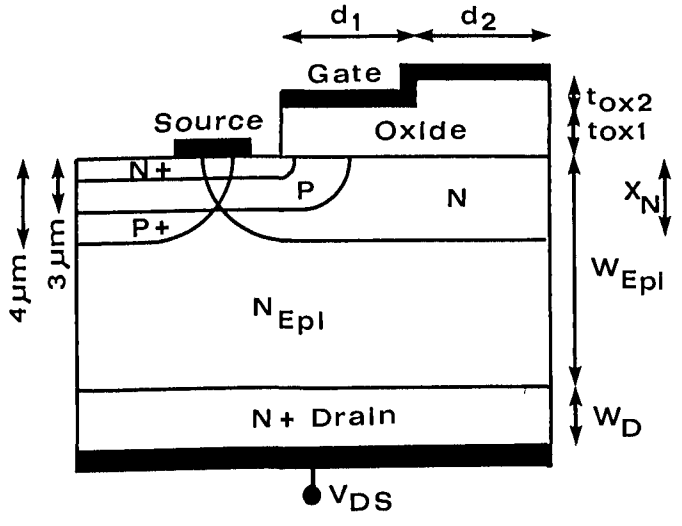

Fig.1 : Cross section of VDMOS structure

The device parameters which are kept constant are given in Table I ; the range of the variable parameters is reported in Table II. The surface concentration of the N-diffusion is limited to the maximum value $N_{SN} = 10^{16} cm^{-3}$ in order to minimize its effect on the threshold voltage. Several combinations of the parameters d_1 and d_2 are considered. We suppose that the device is well protected at the periphery by suitable techniques so that the breakdown does not occur in this region.

TABLE 1

Constant Parameters

N_{epi} (cm^{-3})	N_{SP}^+ (cm^{-3})	N_{SP} (cm^{-3})	t_{ox1} (μm)	W_{epi} (μm)	W_D (μm)
2.8×10^{14}	2.0×10^{18}	2.0×10^{17}	0.1	25	10

TABLE 2

Variable Parameters

t_{ox2} (μm)	0	0.1		0.2		0.4			0.6		
d (μm)	4	6		8		10					
d_1 (μm)	3	3	4	4	6	4	6	8			
d_2 (μm)	1	3	2	4	2	6	4	2			
X_N (μm)	1	2		3		4			5	6	7
N_{SN} cm^{-3}	10^{15}	10^{16}									

3. Numerical method

The breakdown voltage is obtained by two-dimensionnal simulation by mean of our finite-difference package CLAC [2] which allows the determination of the potential distribution in reverse-biased p-n junctions. Such a potential distribution is shown in Fig.2.

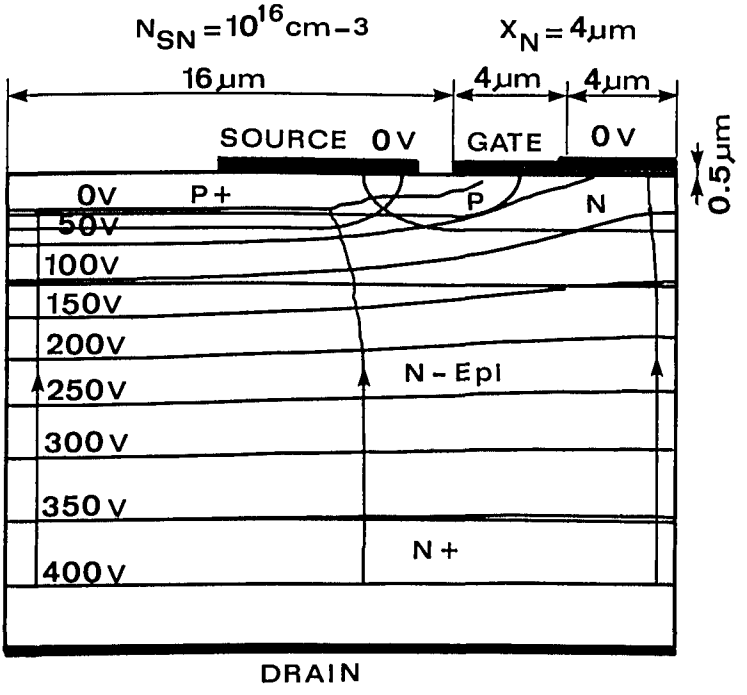

Fig.2 : Potential distribution

The behaviour of the device under high bias V_{DS} is studied by considering three parts. These parts are -the area under the plane part of the junction between the channel zone and the N_{epi} layer -the region around the curved portion of this junction -the middle of the structure. The hole ionization integrale is computed along field lines in these three parts ; the coefficients of VAN OVERSTRAETEN and De MAN are used [3]. The breakdown voltage BV of the device is obtained when the ionization integrale is equal to 1 in one of these parts.

The epitaxial resistance is computed by mean of the distributed resistance network as depicted in Fig.3 [4]. For a structure with a depth of 1 cm the resistance between the modes i and j is given by

$$R_{i,j} = \frac{\rho_i + \rho_j}{2} \qquad (1)$$

where ρ_i and ρ_j are the resistivity at the nodes i and j respectively. At the node i, the resistivity is related to the doping concentration N_i by

$$\rho_i = \frac{1}{q\ \mu_n\ N_i} \qquad (2)$$

The variation of the electron mobility μ_n with the doping concentration is considered [5].

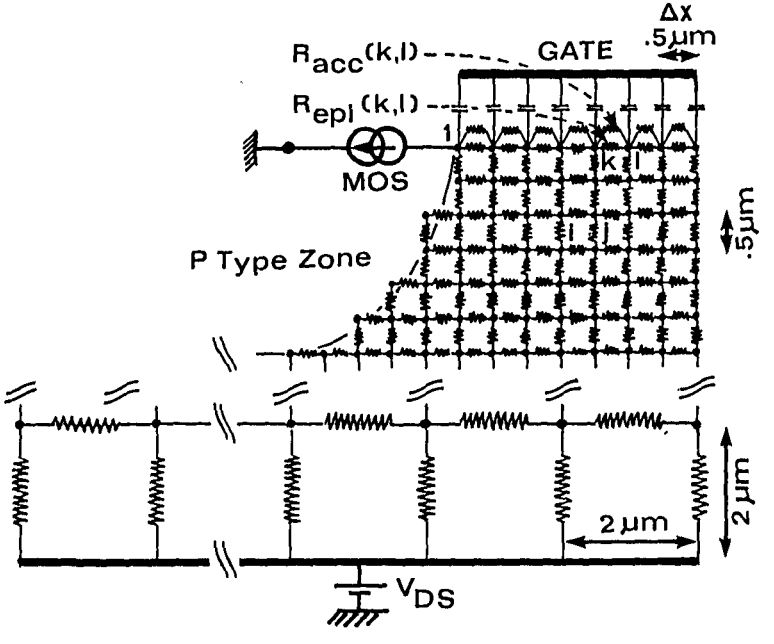

Fig.3 : Resistance capacitance network for the determination of Epi-layer resistance

The electric charge in the accumulation layer at the Si-SiO_2 interface in the N_{epi} region for positive gate bias is computed by mean of the distributed capacitance network, see Fig.3. At node k this charge is

$$Q_k = C_{ox} (V_G - V_k) \tag{3}$$

with

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox1} + t_{ox2}} \tag{4}$$

Then the resistance from the node k to the node 1 at the interface is

$$R_{k,1} = \frac{\Delta x_{k,1}}{\mu_n \frac{Q_k + Q_1}{2}} \tag{5}$$

where $\Delta x_{k,1}$ is the distance from the node k to the node 1.

The elementary accumulation resistances are combined in parallel with the N_{epi} resistances along the Si-SiO_2 interface.

4. Results

The effect of the depth X_N and surface concentration N_{SN} on the breakdown voltage is shown in Fig.4.a) for structures characterized by different distances d. The correspondent variations of the resistance R_{ON} of the epi-layer are plotted in (Fig.4.b). In the $X_N = 0$ case the surface concentration $N_{SN} = 0$. Due to the low impurity concentration in the N_{epi} layer, the channel resistance is neglected [1]. The resistance R_{ON} is [1]

$$R_{ON} = R_{ACC} + R_{JFET} + R_{BULK} \tag{6}$$

A drastic decreasing for the breakdown voltage is obtained for the structures having $N_{SN} = 10^{16}cm^{-3}$ when X_N is increased. Comparing the two cases d = 10 µm, $N_{SN} = 0$ and d = 4 µm, $N_{SN} = 10^{16}cm^{-3}$, X_N = 4 µm, we obtain identical values for BV and R_{ON} but the capacitance C_{GD} is decreased for the latter. By computing the surface of the gate in front of the N_{epi} layer we obtain

$$C_{GD}(d=4\mu m) = \frac{1}{5} \times C_{GD} \ (d=10\ \mu m)$$

The resistance R_{ON} can be further decreased at the expense of BV by making the N-diffusion deeper and by increasing d. A shifting is observed for the location of the breakdown in the

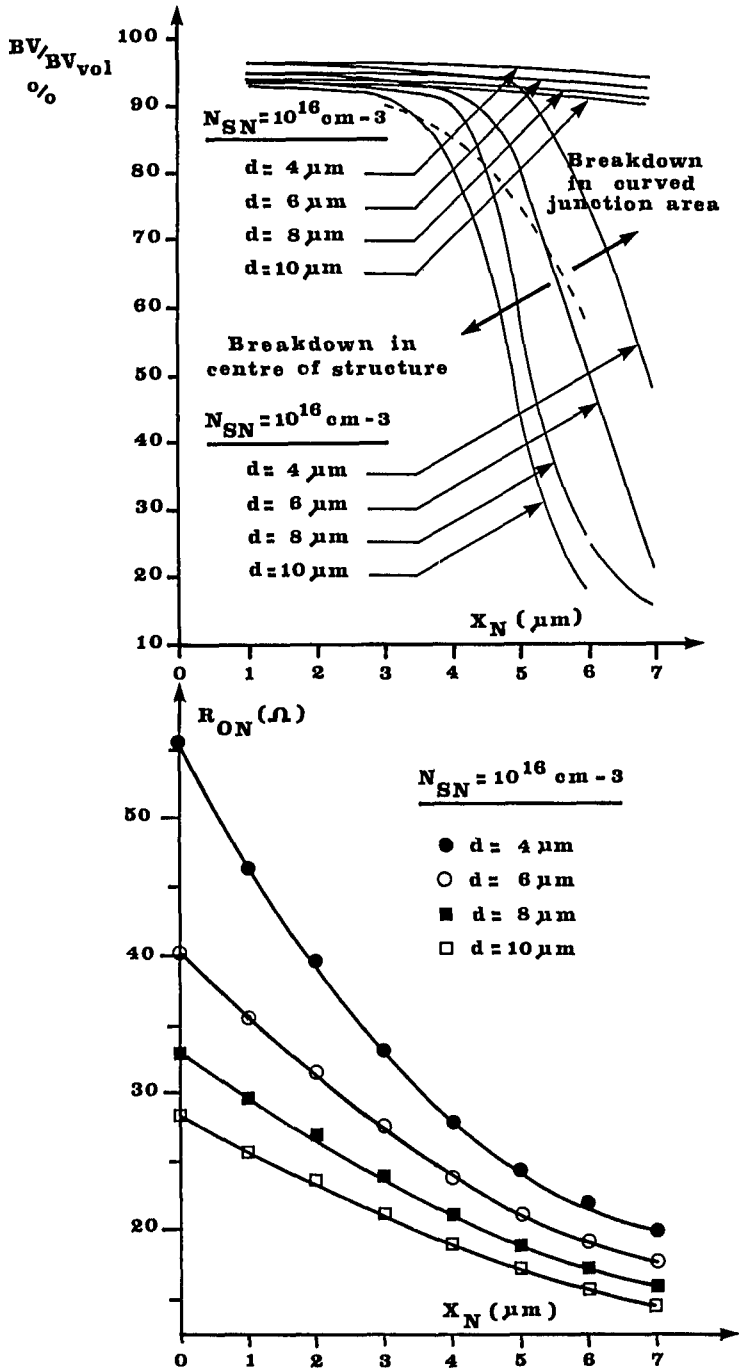

Fig.4 : a) Normalized breakdown voltage
b) Resistance of Epi-layer versus the N-diffusion depth

device. This location moves from the curved junction area when $N_{SN} = 10^{15}cm^{-3}$ to the middle part of the structure when X_N is increased with $N_{SN} = 10^{16}cm^{-3}$. The dashed line in Fig.4.a) corresponds to the simultaneous breakdown in the middle part and in the curved junction area.

Nevertheless the gain obtained for R_{ON} when $N_{SN} = 10^{16}cm^{-3}$ and $X_N > 4$ µm can be retained by making $t_{ox2} > 0.1$ µm for the structures exhibiting breakdown in the middle area. Indeed, increasing t_{ox2}, with V_{DS} = cte and V_{GS} = cte, involves a decreasing for the electric field in the oxide in front of the epi-layer and consequently in Silicon, thus providing no breakown in the central area of the device. As t_{ox2} is increased, the equipotential lines are narrowed in the curved part of the junction and thus the breakdown location can be shifted from the middle to the curved junction. The normalized breakdown voltage is plotted versus the step height t_{ox2} in Fig.5 ; as shown there is an optimum value for t_{ox2} which gives the maximum breakdown voltage. As

$$C_{GD} \propto C_{ox} = \frac{\epsilon_{ox}}{t_{ox1} + t_{ox2}} \qquad (7)$$

the best R_{ON}-BV-C_{GD} tradeoff is obtained when t_{ox2} is optimum.

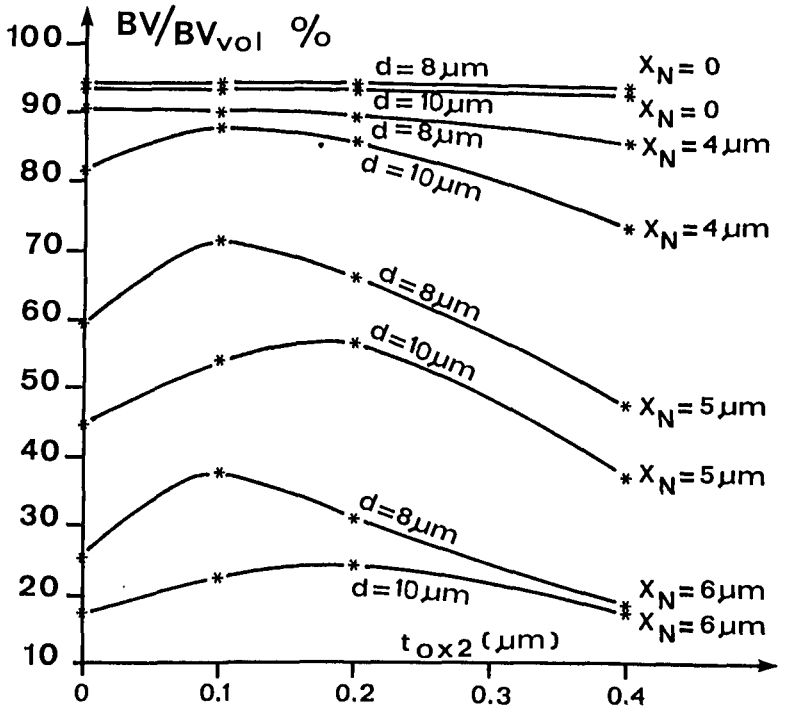

Fig.5 : Normalized breakdown voltage versus the oxide step height

For instance consider a structure with d = 10 µm, t_{ox2} = 0,1 µm, and compare BV, R_{ON} for structures with $N_{SN} = 10^{16}$ cm^{-3}, X_N = 5 µm and without N-diffusion. We obtain BV/BV_{voi} = 71 %, 95 % and R_{ON} = 16 Ω, 30 Ω respectively, which give a gain for R_{ON} of 50 % while the loss on BV is equal to 25 % approximatively.

5. Conclusion

The tradeoff between R_{ON}, BV and C_{GD} has been studied for power VDMOS transistors by numerical two-dimensionnal simulation and network analysis. A structure with a N diffused zone and an oxide step in its central area, in order to decrease the resistance R_{ON} and the capacitance C_{GD} has been presented. The N-diffusion allows the decreasing of the total area of the device without damaging the resistance R_{ON}. Low values of R_{ON} can be obtained by increasing the surface concentration and the depth of the N-diffusion ; for a given R_{ON}, there is an optimum value of the step oxide height which gives the maximum breakdown voltage.

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