SIMULATION OF THE ISOLATING BEHAVIOUR OF A TRENCH CAPACITOR

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1. SUMMARY

The isolating behaviour of a trench capacitor with respect to a n-channel MOSFET and another trench capacitor has been investigated by 2D numerical simulations, and compared with electrical measurements. The influence of the distance between the MOSFET and the trench capacitor and of the substrate doping density on punch through has been studied. It was found out, that below a critical distance the isolating behaviour of the device is strongly detoriated by the space charge region of the trench. This critical distance decreases for higher substrate doping and increases with higher trench depth. To suppress punch through for distances smaller than 1 µm, one has to adjust properly substrate doping or to use a deep p-well technology.
For the case of two neighboured trench capacitors, a quasi-3D simulation with a realistic shape of the trench has been carried out and compared with conventional 2D simulations. It was found that the results of the conventional simulation overestimates punch through, whereas the quasi-3D simulation agreed very well with the experiments. This kind of simulation was used to study the influence of the distance between two neughbouring trenches and the substrate doping on the punch through voltage.

2. INTRODUCTION

With increasing integration density of DRAM's the device geometry has to be decreased. However, the capacitance must be large enough to have sufficient S/N ratio to guarantee stable circuit operation. For 1 Mbit and 4 Mbit DRAM's the trench capacitor cell structure has been widely investigated /1, 2/, where the capacitor consists of a trench with doped side walls. This concept allows to store enough charge in a cell with small lateral dimensions. However, at extremely small distances between the capacitor and other parts of

the device, punch through may occur when bias is applied, which leads to fast dischargement of the capacitor. In the optimization of geometry and doping profiles of a DRAM cell, the 2D general purpose device simulator GALENE /3/ has been utilized, which allows a quick and reliable calculation of leakage currents for arbitrarily chosen device geometries. At the bottom and the side walls of the trench a Hi C doping was assumed. The doping profile of the source/drain regions and the trench doping was given analytically by Gaussian functions.

3. RESULTS

3.1 Trench capacitor to transistor leakage

In a first step, the isolating behaviour of a trench capacitor against a n-channel MOSFET, whose drain was adjacent to the capacitor, in a homogeneously doped p-substrate has been investigated. Fig.1 shows one of the geometries used in the simulations, defining the distance D between the trench and the channel.

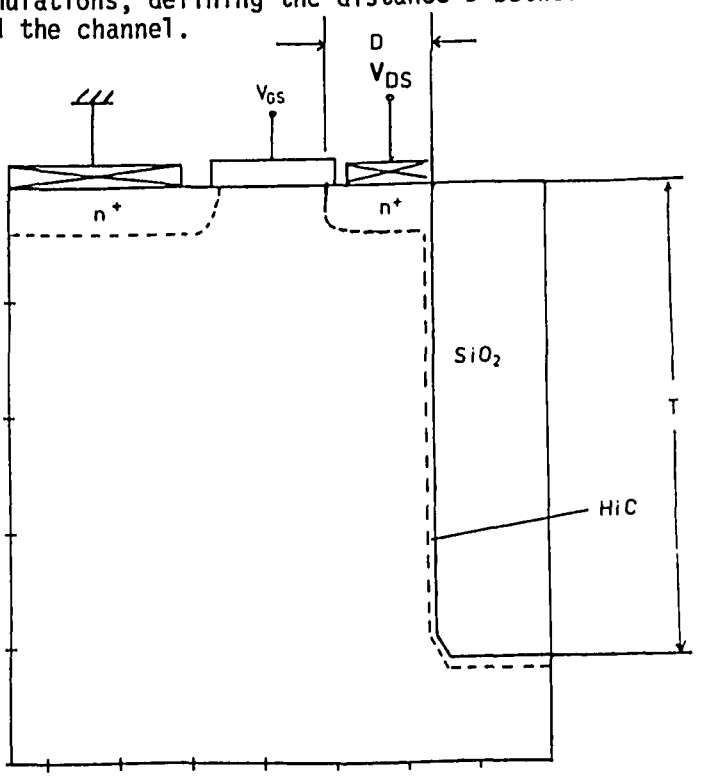

Fig.1: Simulation region, defining the distance D between the capacitor and the channel.

The leakage current between the source and drain contact has been calculated as a function of the applied drain voltage for several distance D and the trench depths 2 and 4 µm, respectively. It was found that for large distances D 2 µm the trench does not influence the isolation between source and drain. When the trench is moved towards the channel, the surfaces of constant drain potential are bent down and towards the channel. The space charge region of the drain/capacitor area may reach the source region as D becomes very small and the drain bias large enough. By assuming a critical leakage current of 1pA/µm and a worst case drain bias of V_{DS} = 7V, the critical distance is found to be 1.2 µm for the trench depth T = 2 µm, and 1.3 µm for T = 4 µm, respectively. This result shows that for trench depths larger than 2 µm the depth is of minor influence on the leakage current. To adjust the doping profile in such a way to suppress punch through effectively even for extremely small distances D, we studied the current path by plotting the current densities. Fig.2 shows the electron current density for D = 0.7 µm and V_{DS} = 5V. The trench depth

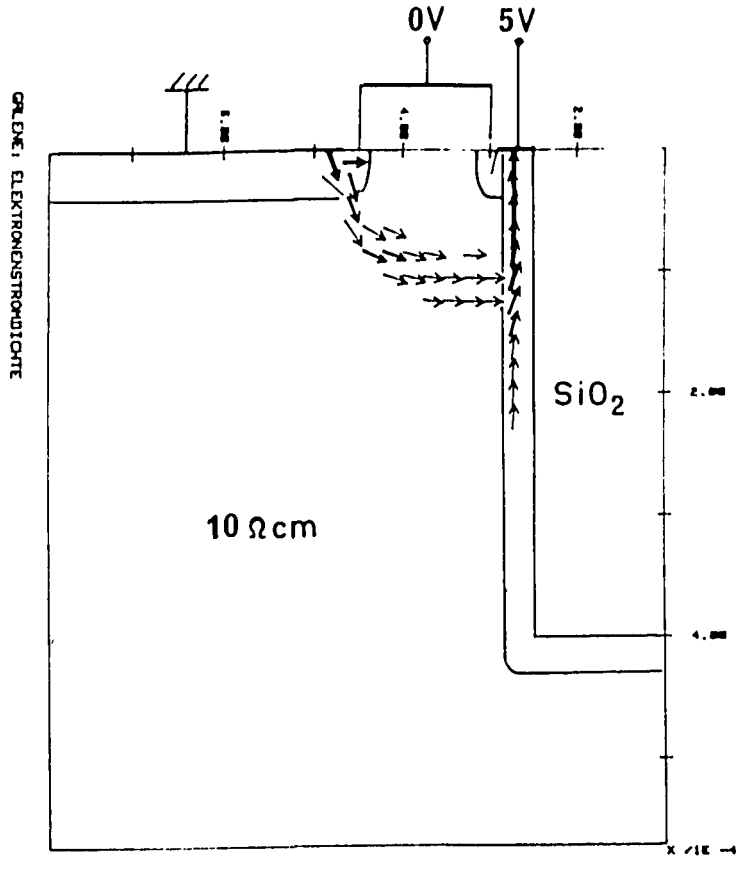

Fig.2: Electron current density for D=0.7 µm and V_{DS}= 5V.

is assumed to be 4 µm, the effective channel length about 1.2 µm. One can see that for submicron distances most of the current flows directly to the trench doping. The current path is in a depth of about 1 µm. By increasing the substrate doping to 7E15 cm^{-3} punch through is suppressed effectively, even for distances smaller than 0.7 µm. If a p-well technology is used, the depth of the well has to be about 2 µm. On the other hand, the well must not increase the doping concentration at the surface significantly to avoid a threshold voltage shift. Simulations with p-well profiles convenient for n-channel MOSFET's /4/ indicate that a deep p-well can be used to suppress punch through between the capacitor and the MOSFET.

3.2 Trench to trench leakage

Another isolation problem related to the trench cell concept is the punch through between two neighbouring trench capacitors under bias conditions. This problem seems to be much more serious, because the capacitors of width W and depth T are like two parallel plates of a capacitor, separated by a distance of approximately $D-2x_j$, where D is the distance between the trenches, and x_j is the junction depth of the side wall doping. In a conventional 2D simulation the third dimension along the z-axis is assumed to be infinitely large compared with the other two dimensions of the device. Using the 2D simulator GALENE, such a calculation has been done for two trench capacitors of 3 µm depth. The distance between the trenches was D = 1.8 µm. For the doping profiles, again Gaussian distributions have been assumed with a junction depth of 0.1 µm. The impurity density of the homogeneously doped p-substrate was varied from 7E15 to 5E16 cm^{-3}. The difference of the electrostatic potential between the capacitors was 5V. It was found that a minimum substrate doping of 5E16 cm^{-3} is necessary to keep the leakage current below 1pA. This result is only valid for very large trench geometries. It overestimates the leakage current considerably if finite 3D geometries, e.g. cylindrical trenches are used. To study the influence of the third dimension, another 2D simulation has been done, using the same simulator, but choosing the simulation region parallel to the silicon surface, as shown in Fig.3. As indicated by REM photographs,

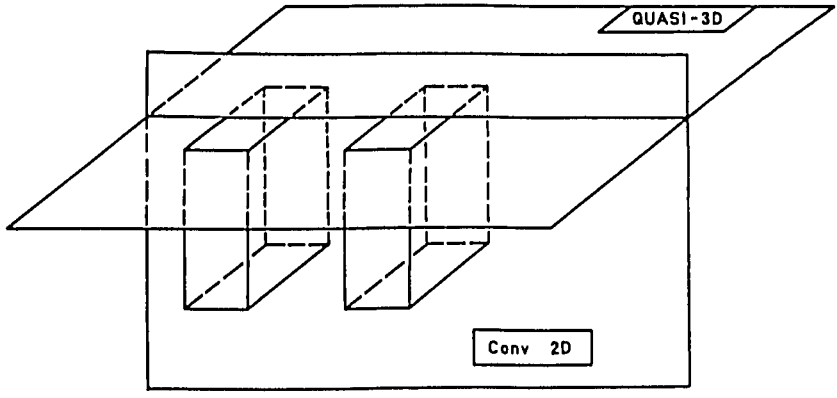

Fig 3 Cutting planes, defining the simulation region

a rectangle with rounded corners has been assumed for the cross section of the trenches. The necessary assumption for this kind of simulation is an infinitely deep trench, which seems to be more realistic for this problem than that of two parallel capacitor plates of infinitely large dimension in z-direction. The distance between the trenches and the doping profiles were the same as above. Fig.4 shows the results of this so-called quasi-3D simulation compared with the conventional one, and the measured data.

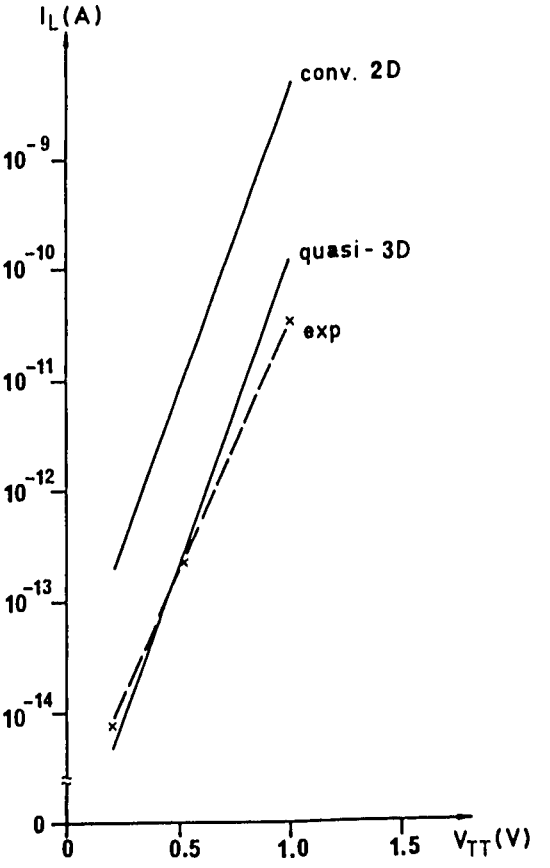

Fig. 4: Comparison of the simulated leakage currents with the experiment for D = 1.8µm and V_{Sub} = 0V

It indicates that the simulation plane in a 2D simulation has to be chosen carefully with respect to the physical problem. By this suitable choice of the simulation region it seems to be possible to investigate the electrical behaviour of a highly 3D structure, like the trench cell, by a 2D device simulator. Fig.5 shows the potential distribution resulting from the quasi-3D simulation for V_{TT} = 0.6V, where the leakage current reaches 1pA.

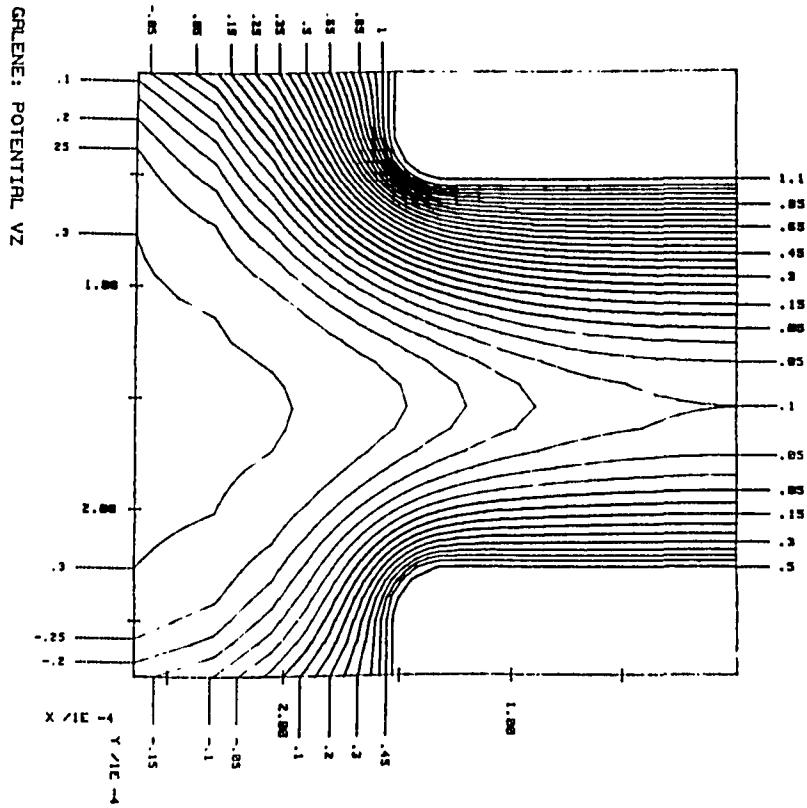

Fig.5: Potential distribution (quasi-3D) for V_{TT} = 0.6V.

For this simulation, the cross section of the trench was 3/um x 1/um.

References:

1. SUNAMI, H. et.al.
"A corrugated capacitor cell for megabit dynamic MOS memories"
IEDM Tech. Dig. Vol. , p. 806, 1982

2. MORIE, T., MINEGESHI, K. and NAKAJIMA, S.
"Depletion trench capacitor technology for megabit level MOS DRAM"
IEEE Electron Device Leff., Vol. EDL-4, p. 411, 1983

3. ENGL, W.L., DIRKS, H.K. and MEINERZHAGEN, B.
"Device Modeling"
Proc. of the IEEE, Vol. 71, p. 10, 1983

4. RISCH, L., WERNER, C., MÜLLER, W. and WIEDER, A.
"Deep-Implant 1 µm MOSFET Structure with Improved Threshold Control for VLSI Circuitry"
IEEE Trans. Electron Devices, Vol. ED-29, p. 601, 1982